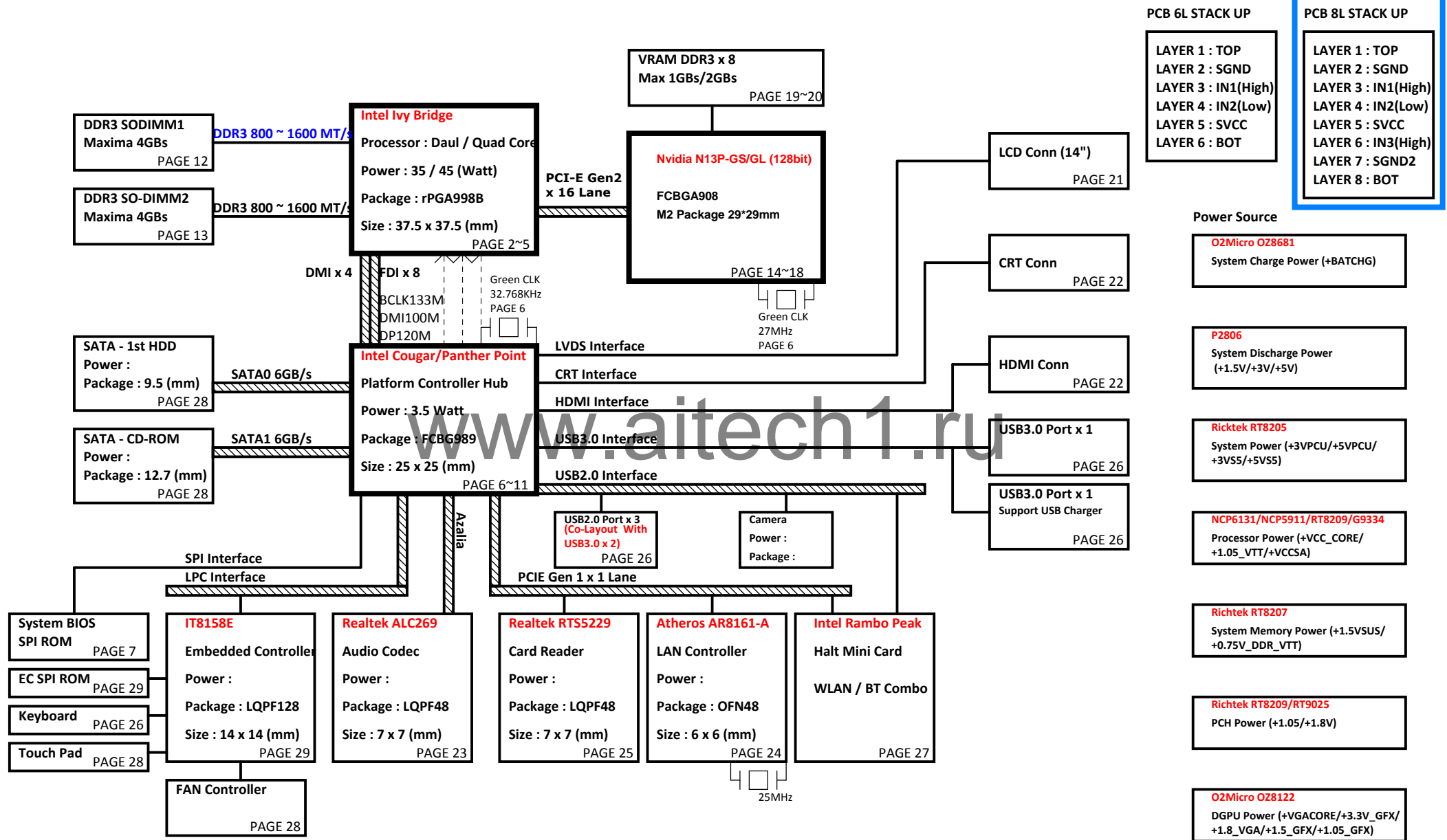
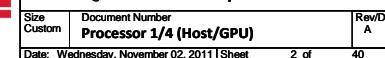
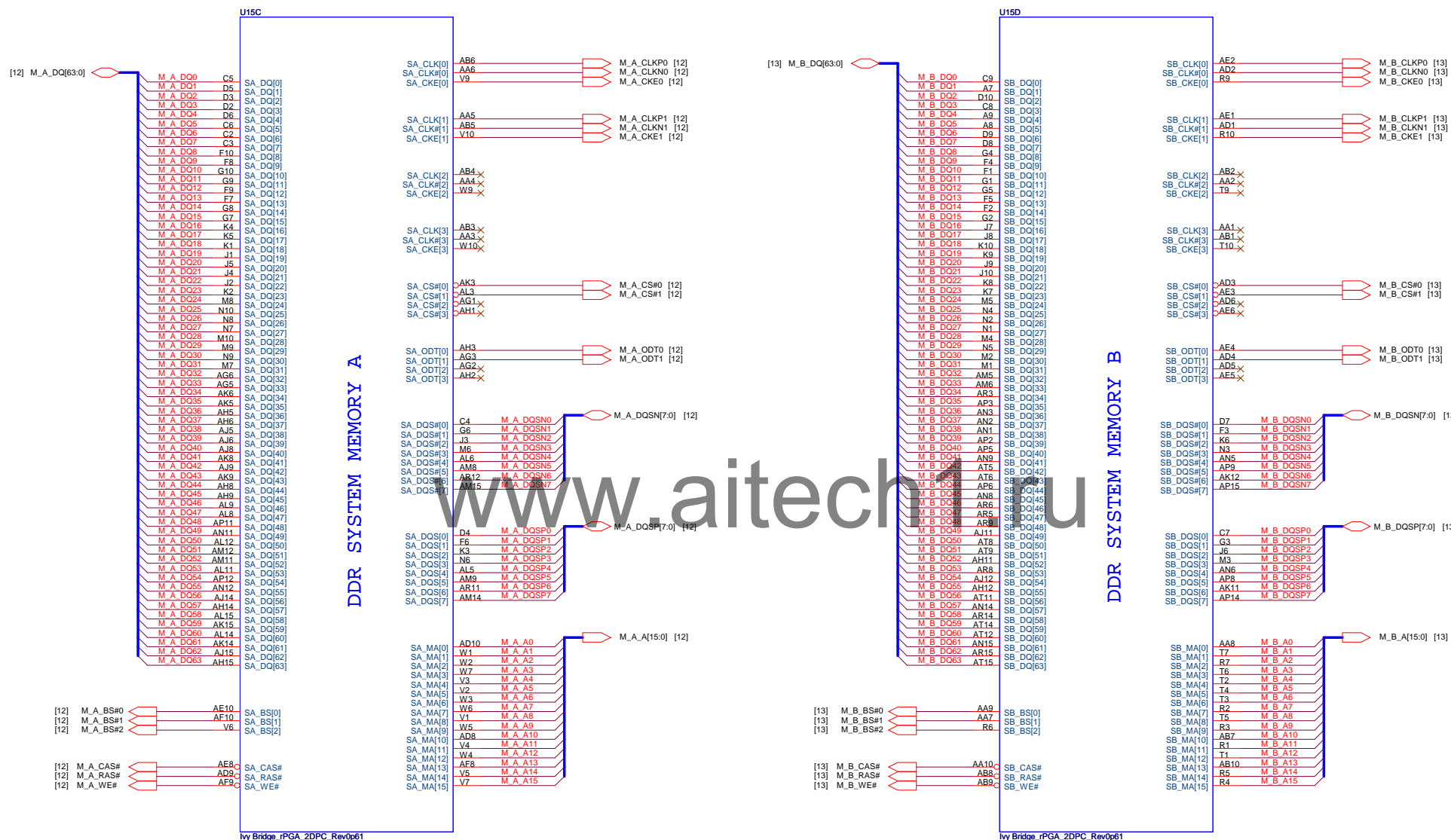


JW2 DIS (14") Intel Chief River Platform Block Diagram 01



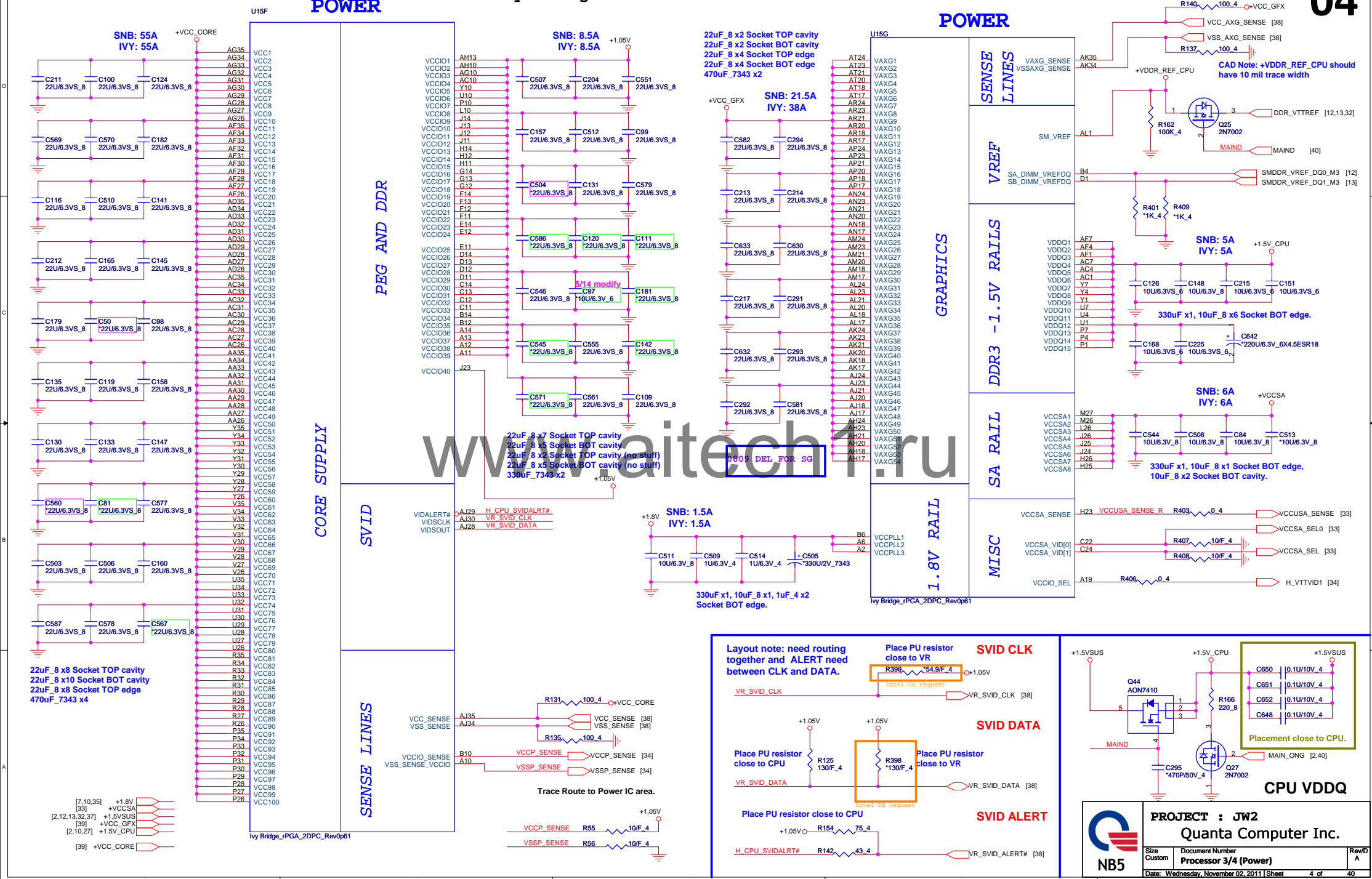


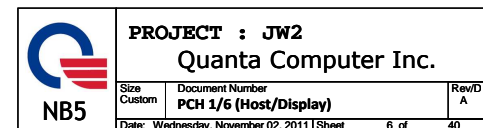
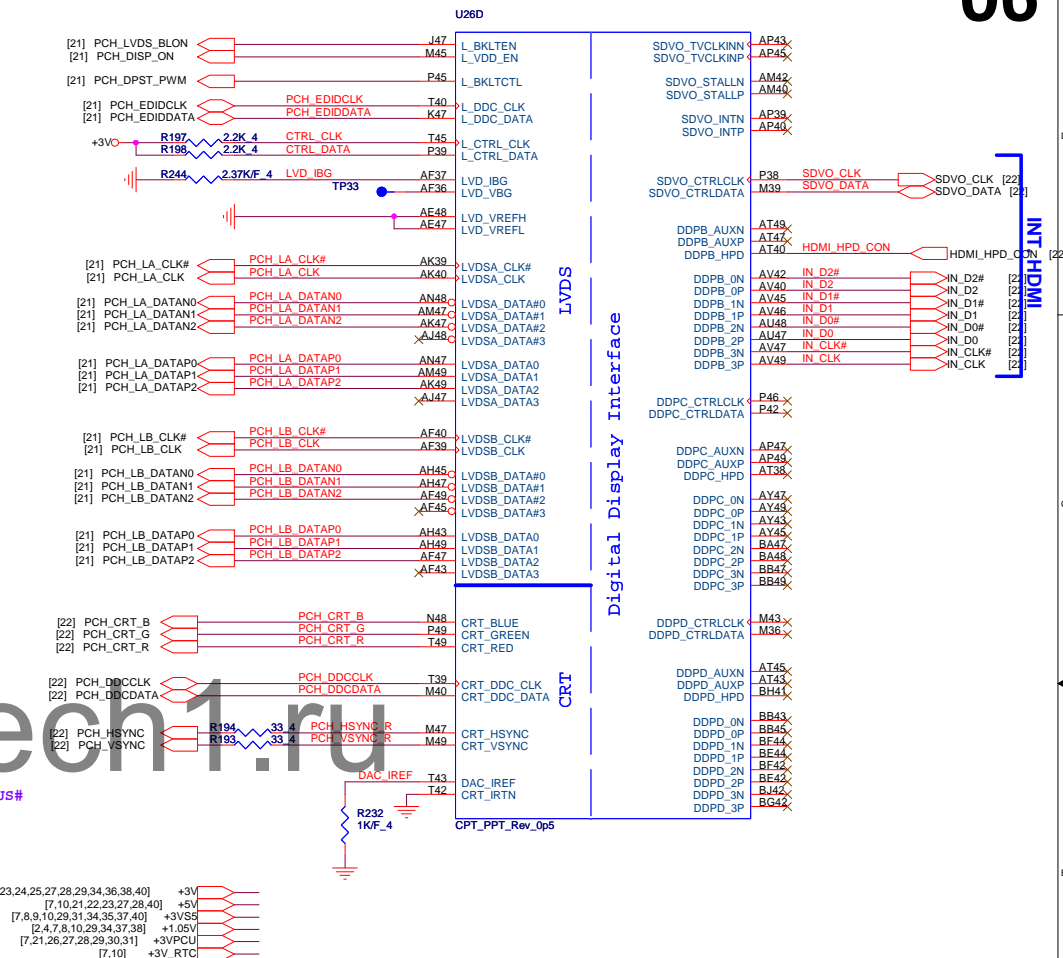
Ivy Bridge Processor (DDR3)



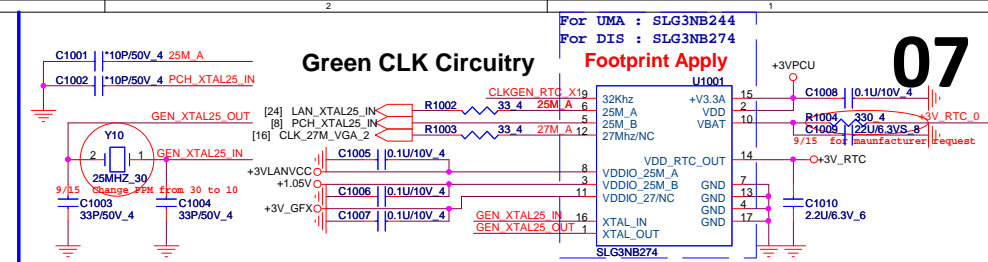
POWER

POWER





07



ODD (SATA1 6Gb/s)

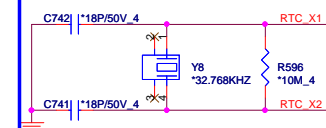
Green CLK Circuitry

Footprint Apply

30mils

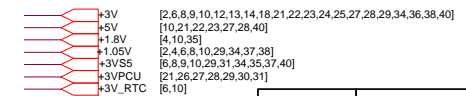


RTC Clock 32.768KHz



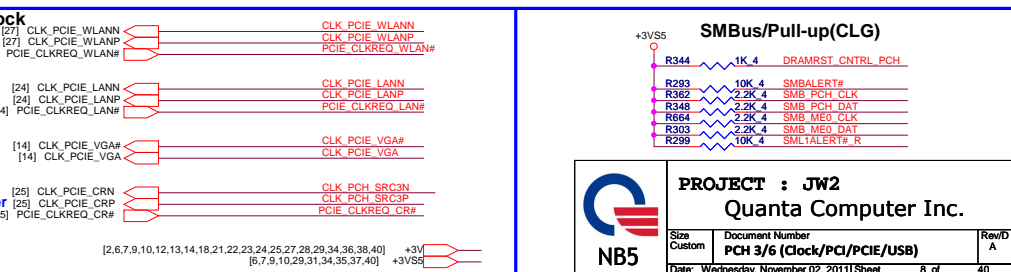
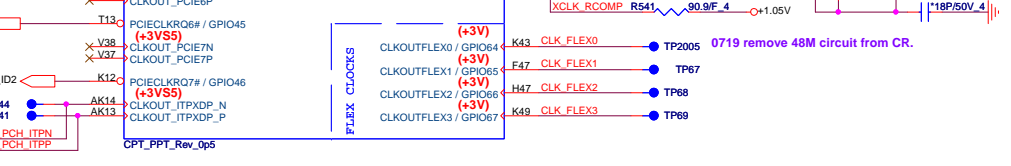
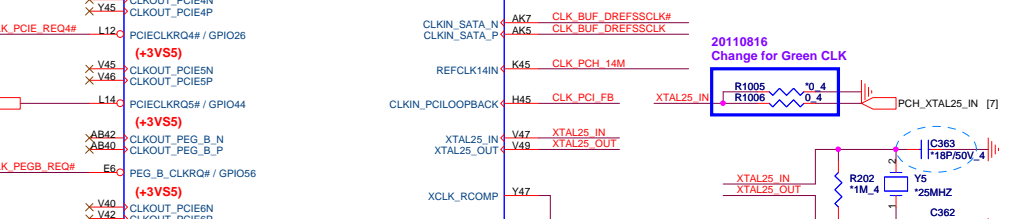
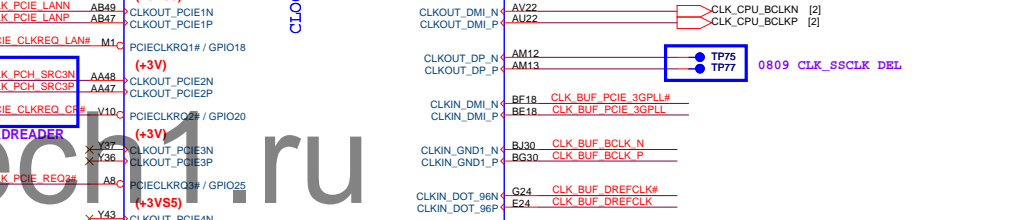
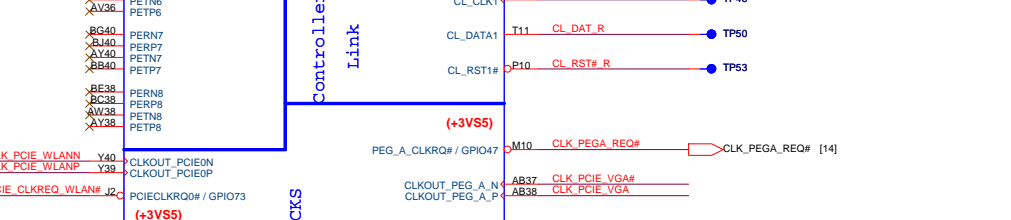
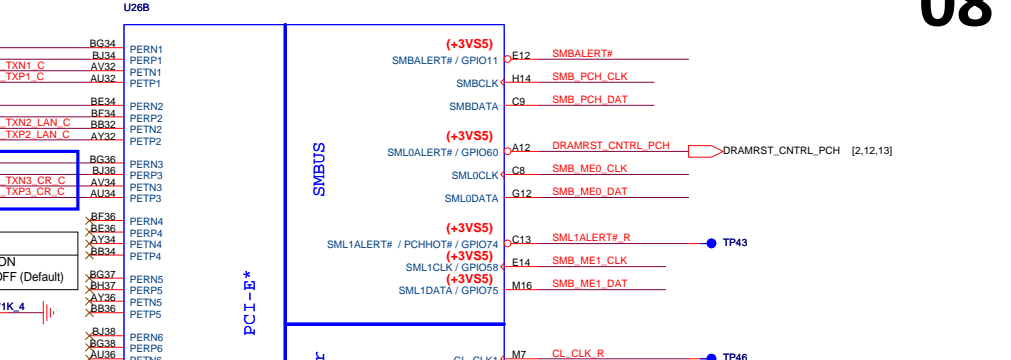
Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR <i>Different from Calpella</i>	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security <i>Only for Interposer</i>	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr> </thead> <tbody> <tr> <td>1</td><td>0</td><td>SPI</td></tr> <tr> <td>0</td><td>0</td><td>LPC</td></tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	1	0	SPI	0	0	LPC	<p>(Need external pull-down for LPC BIOS) Default weak pull-up on GNT0/1#</p>
GNT1#	GNT0#	Boot Location											
1	0	SPI											
0	0	LPC											
GPIO19 <i>Different from Calpella</i>	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
NV_ALE	Intel Anti-Theft HDD protection <i>Only for Interposer</i>	PWROK	0 = Disable (Internal pull-down 20kohm)										
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
GPIO28 <i>Different from Calpella</i>	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										

PCH SPI ROM(CLG)

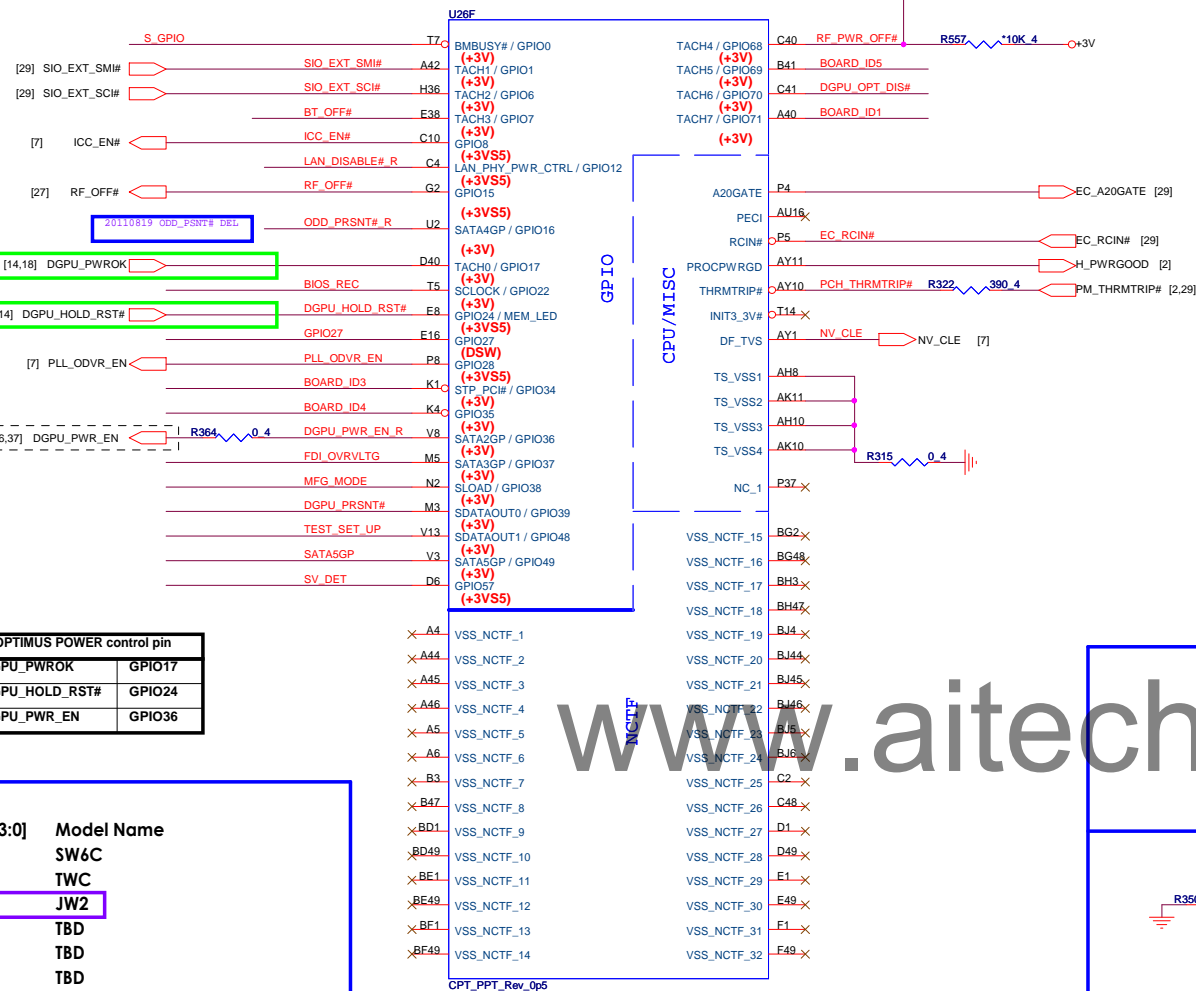


Size Custom	Document Number PCH 2/6 (HDA/RTC/SATA/SPI)	Rev A
Date: Wednesday, November 02, 2011 Sheet 7 of 40		

Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



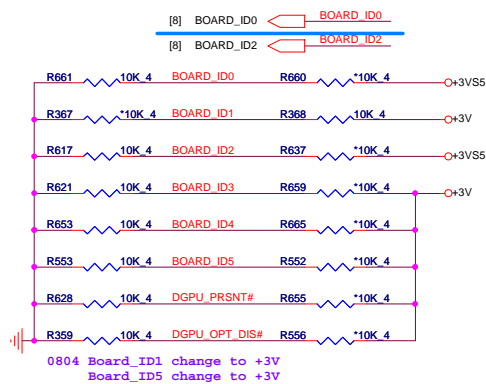
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



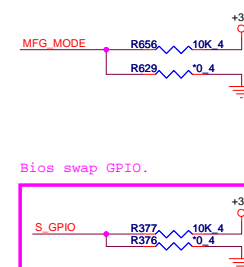
Chief River BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO71	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO34	MODEL BIT3
BOARD_ID4	GPIO35	No Dolby=0, Dolby=1
BOARD_ID5	GPIO69	Reserve and pull low
DGPU_PRST#	GPIO39	Reserve and pull low
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1

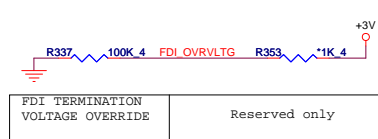
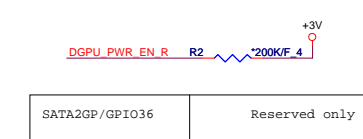
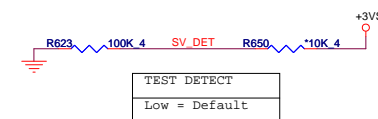
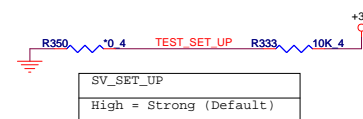
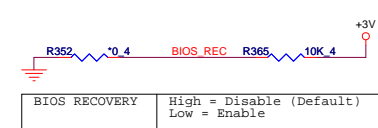
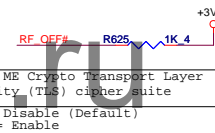
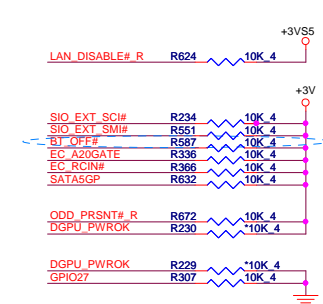
20110816 Define BRD_ID[3:0]



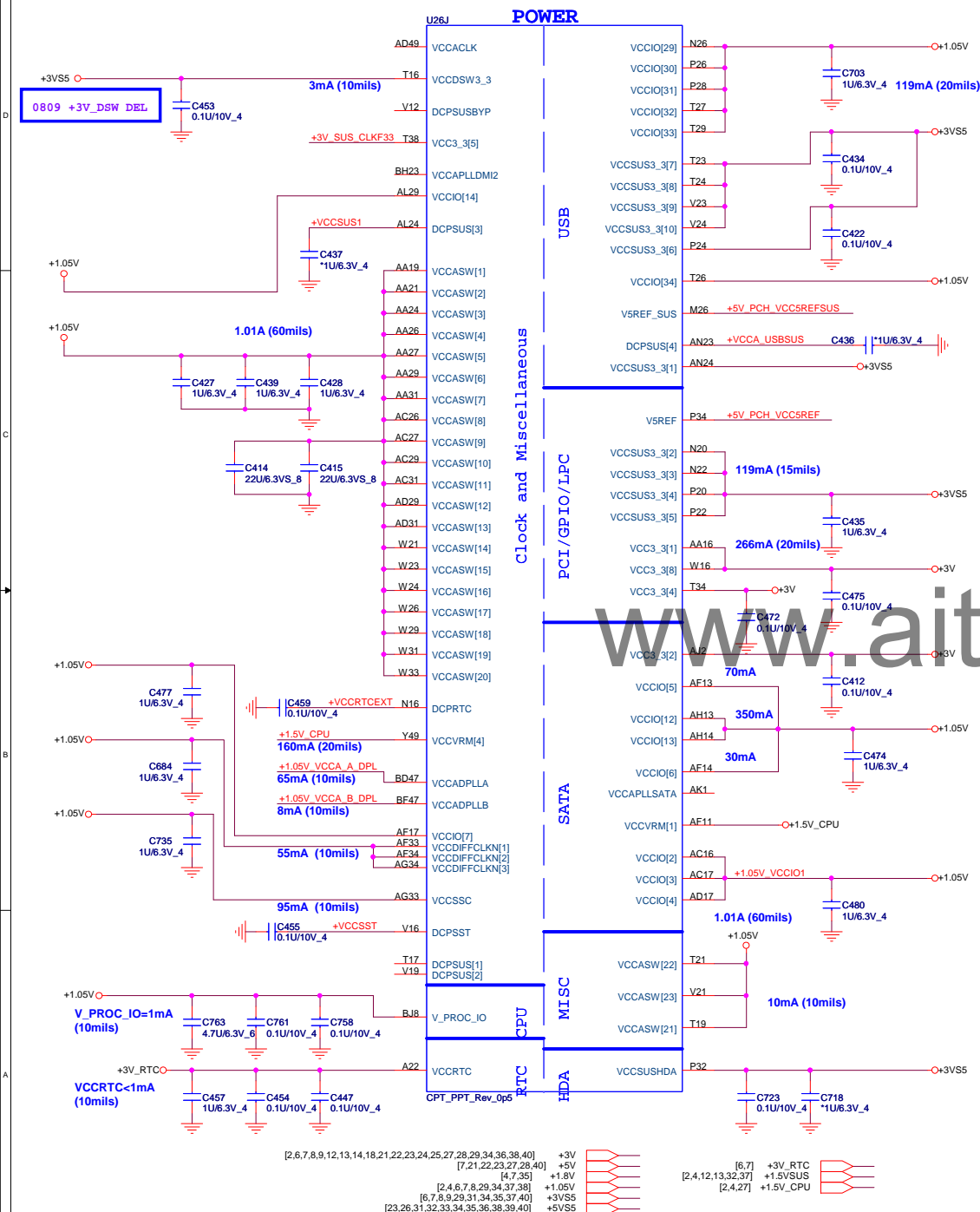
MFG-TEST



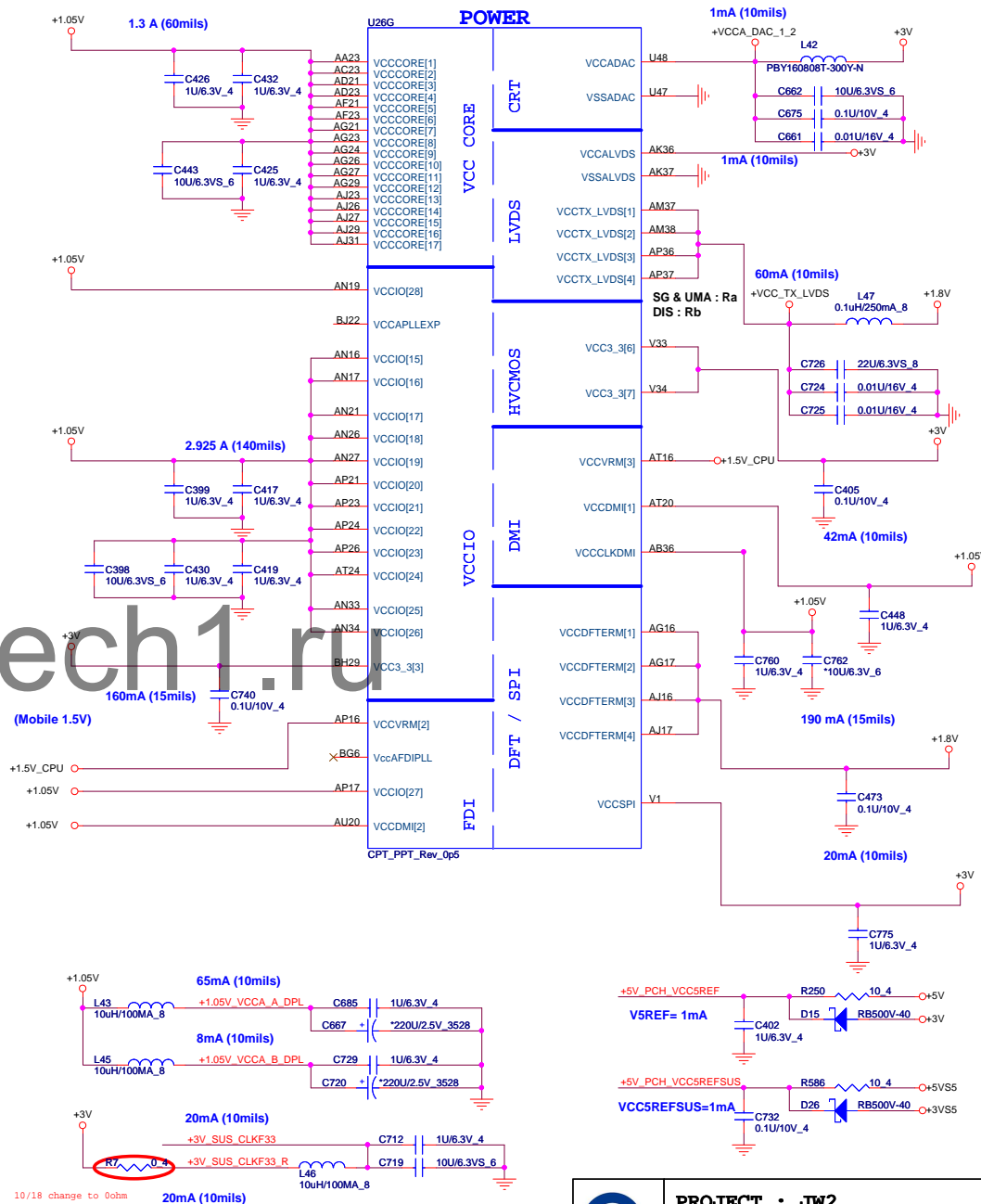
GPIO Pull-up/Pull-down(CLG)



Cougar Point/Panther Point (POWER)

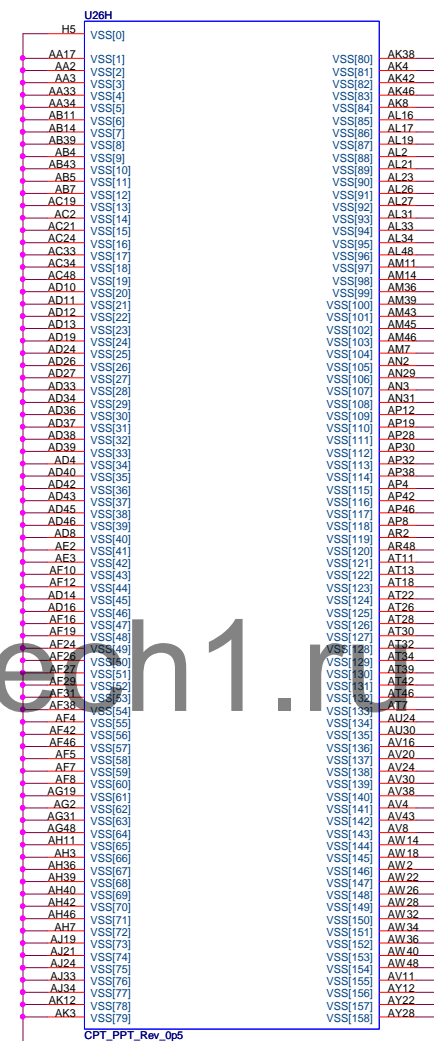
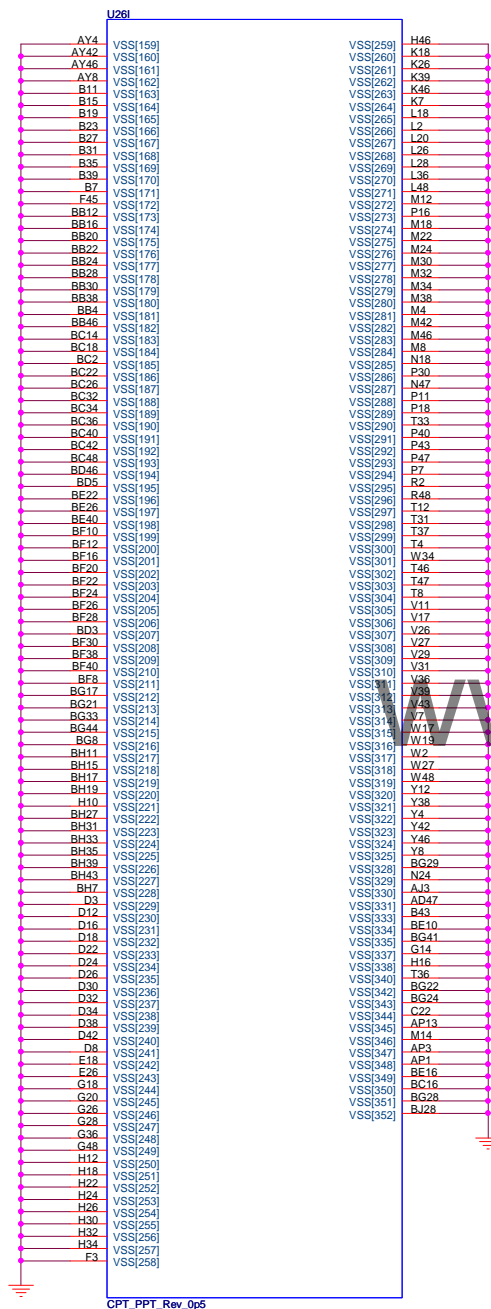


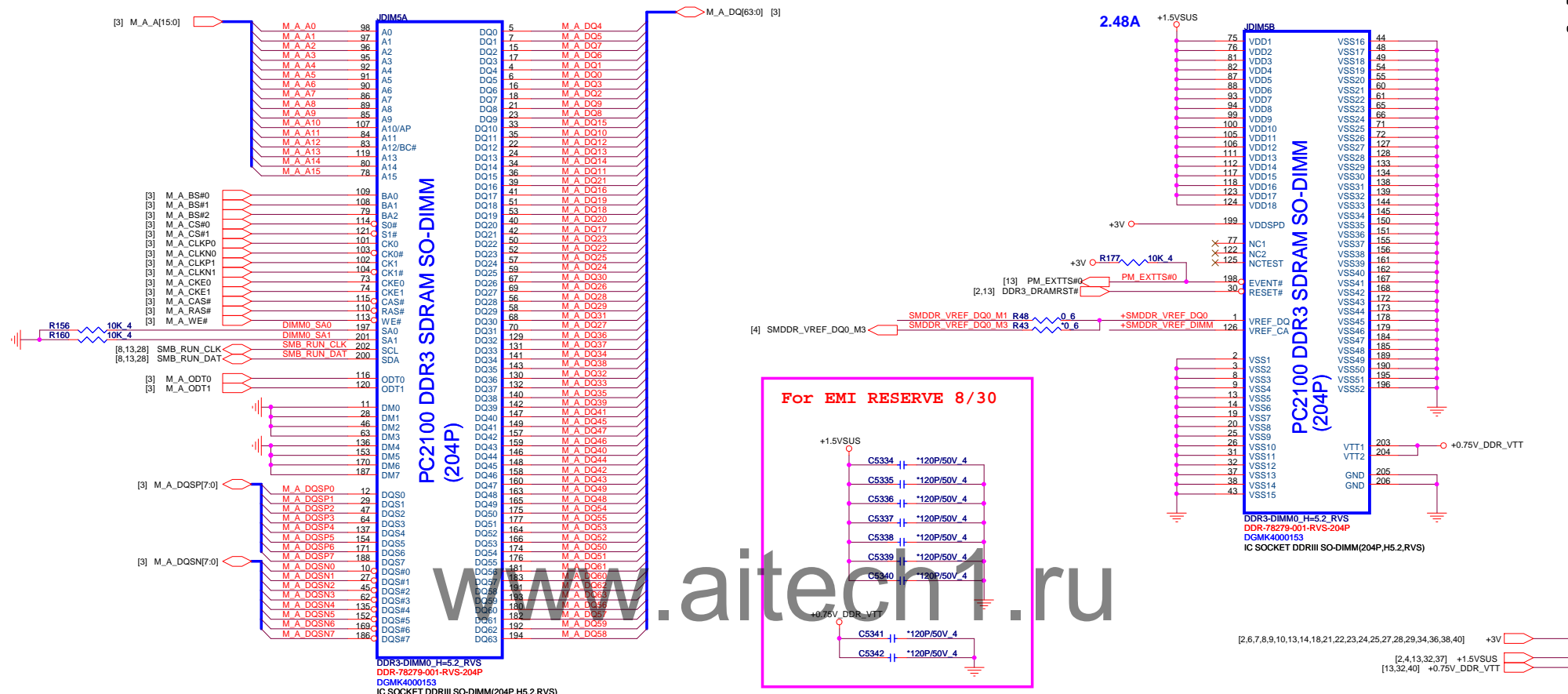
Cougar Point/Panther Point (POWER)



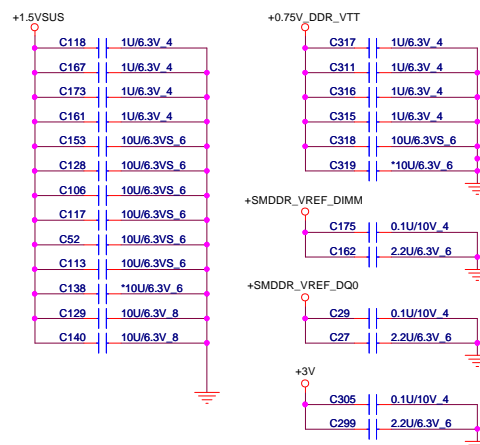
Cougar Point/Panther Point (GND)

Cougar Point/Panther Point (GND)

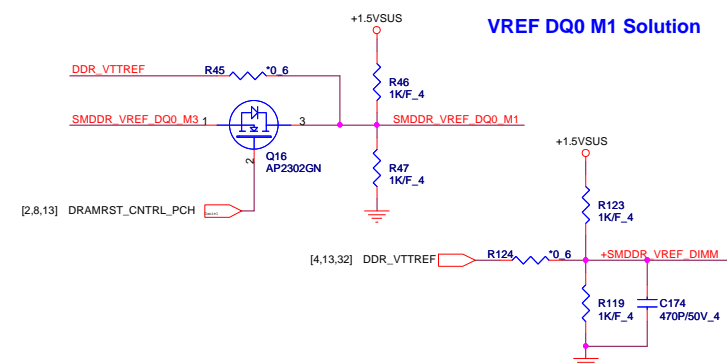


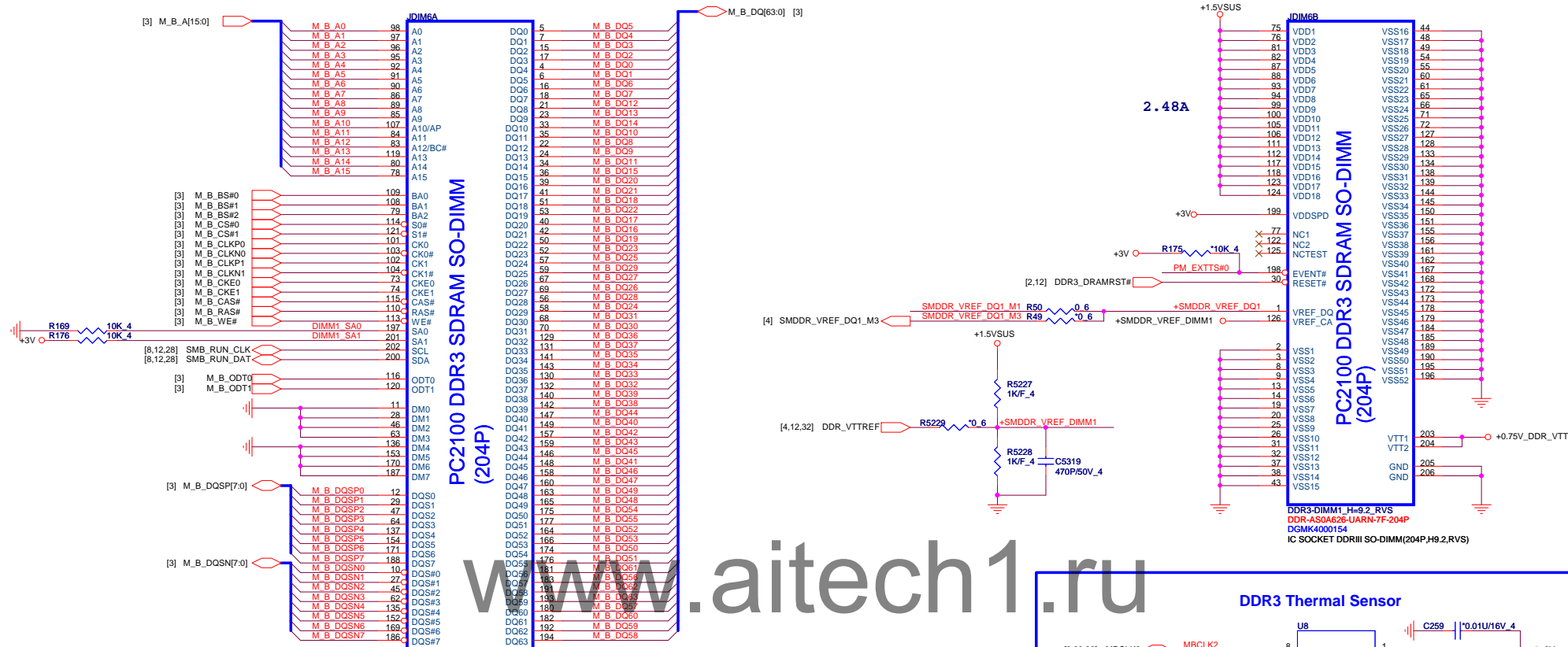


Place these Caps near So-Dimm0.

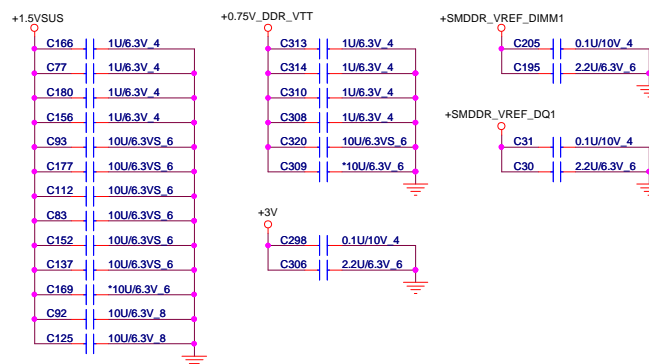


VREF DQ0 M1 Solution

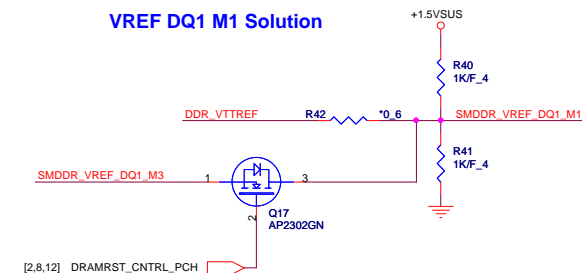


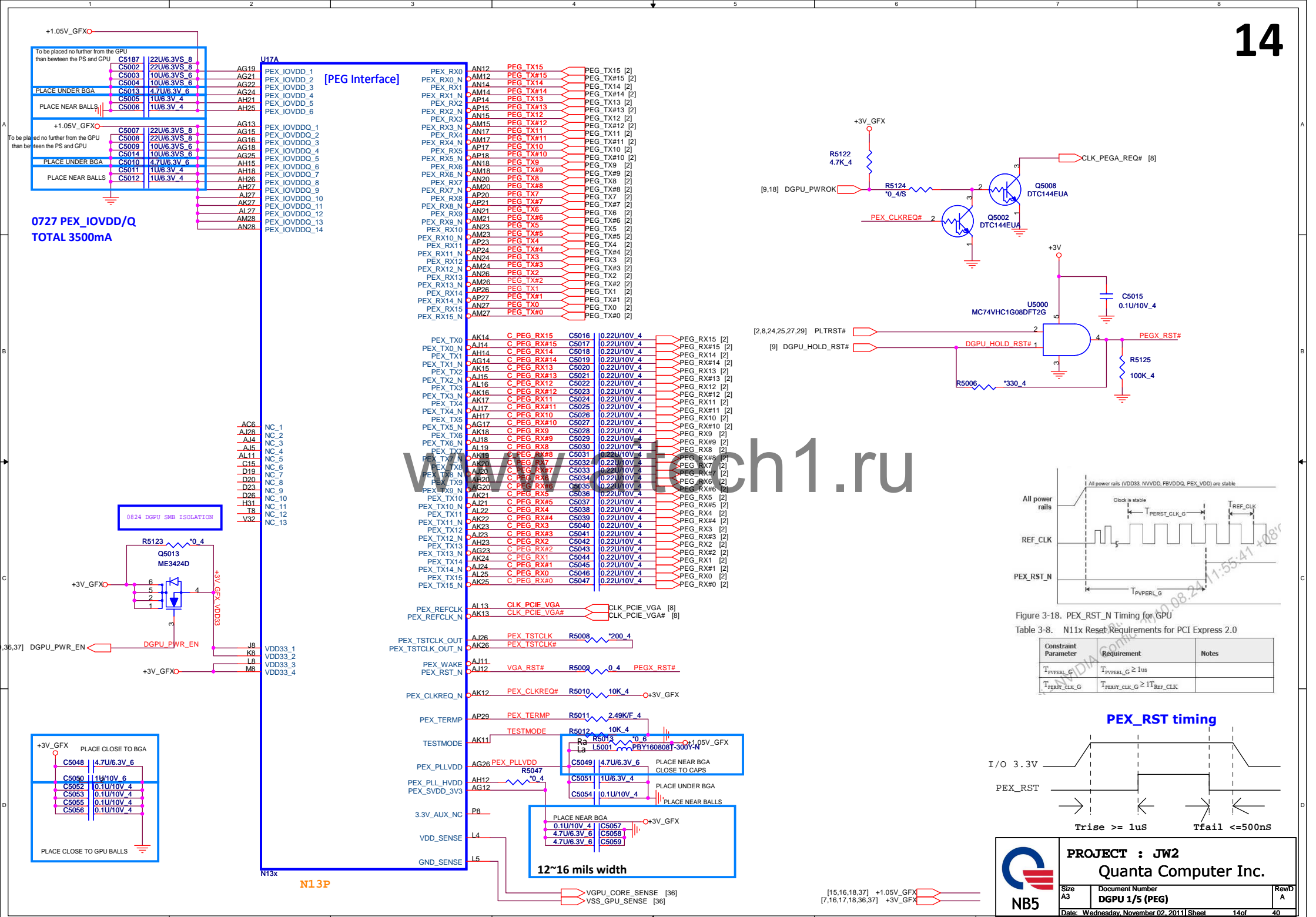


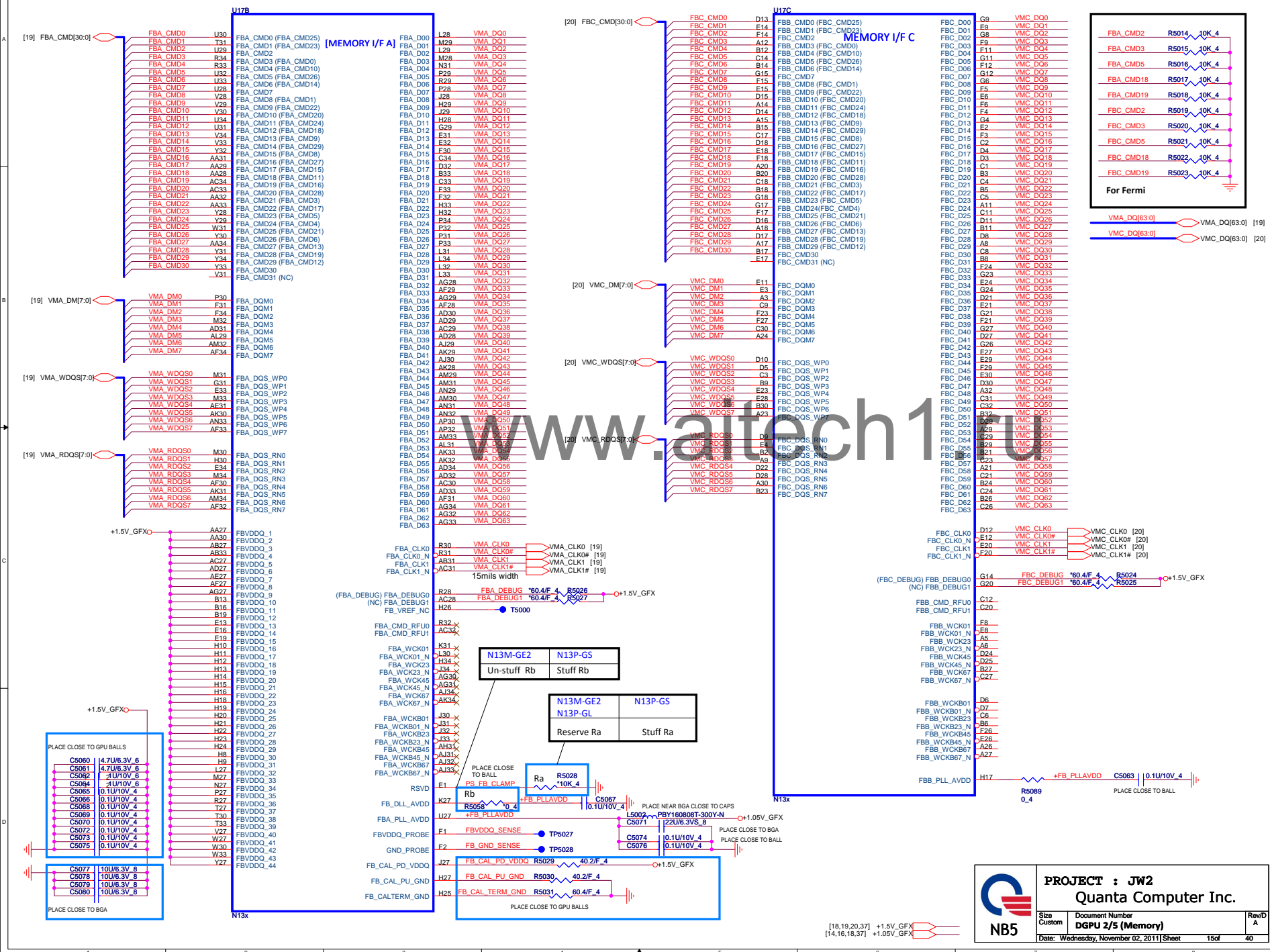
Place these Caps near So-Dimm1.

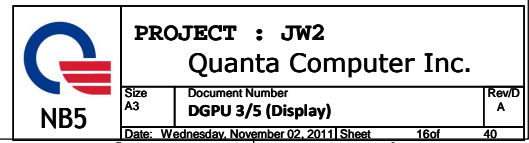


VREF DQ1 M1 Solution







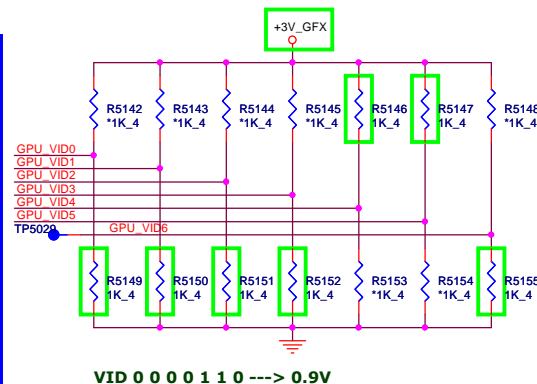


Net name	N13M-GE2	N13P-GS (QS)
ROM_SI		
ROM_SO	PD 10K	PU 5K
ROM_SCLK	PD 15K	PD 10K
STRAP0	PU 45K	PU 45K
STRAP1	PD 35K	PD 35K
STRAP2	PU 15K	PD 15K
STRAP3	UN-STUFF	PD 5K
STRAP4	UN-STUFF	PD 10K

For N13M-GE2
ROM_SO PD 10K
ROM_SCLK PD 15K

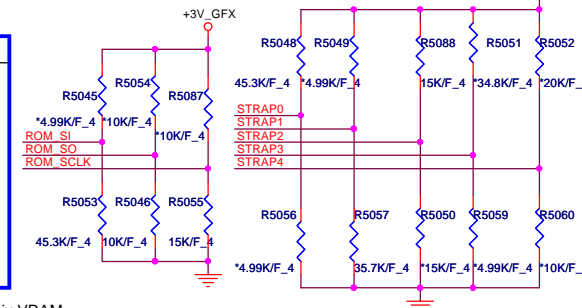
For N13M-GS (QS)
STRAP3 PD 5K
STRAP4 PD 10K
ROM_SCLK PD 10K

N13M-GE2-A1 ID:0X0DEA
N13P-GS ID:0X0FD2



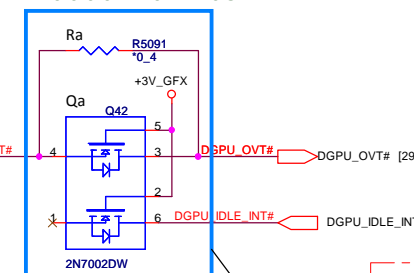
Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



Default: Hynix VRAM

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	1001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0011
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0111
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	XXXX
STRAP4	RESERVED	PCI SPEED CHANGE GEN3	PCI_MAX SPEED	DP_PLL_VDD33	XXXX



	N13M-GE2	N13P-GS
Ra	Un-Stuff	Stuff
Qa	Stuff	Un-Stuff

For N13M-GE2, N13M-GS (QS)
Default : 2G Samsung

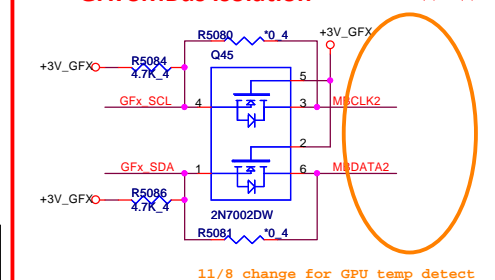
VRAM Configuration Table

ROM_SI	
1G Hynix 64Mx16	-->15K PD
1G Samsung 64Mx16	-->20K PD
2G Hynix 128Mx16	-->35K PD
2G Samsung 128Mx16	-->45K PD

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	OUT	GPU_VID4	GPU CORE_VDD VID4
1	OUT	GPU_VID3	GPU CORE_VDD VID3
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	GPU_VID1	GPU CORE_VDD VID1
6	OUT	GPU_VID2	GPU CORE_VDD VID2
7	OUT	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF	MEMORY VREF CONTROL
11	OUT	GPU_VID0	GPU CORE_VDD VID0
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	GPU_VID5	GPU CORE_VDD VID5
14	IN	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	MEM VDD	MEMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	

GFx SMBus Isolation



11/8 change for GPU temp detect

	N13M-GE2	N13P-GS
Stuff Rc		Un-stuff Rc



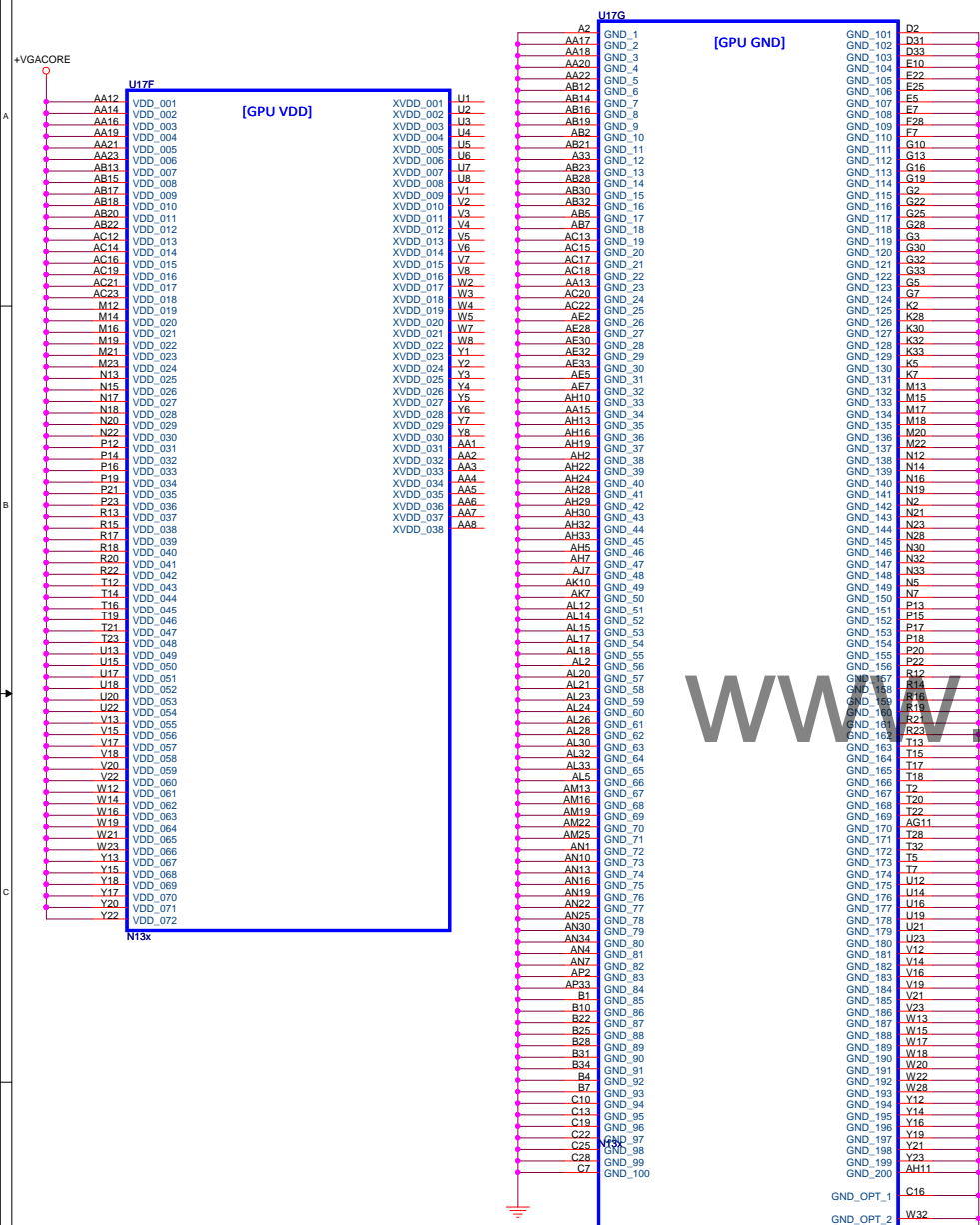
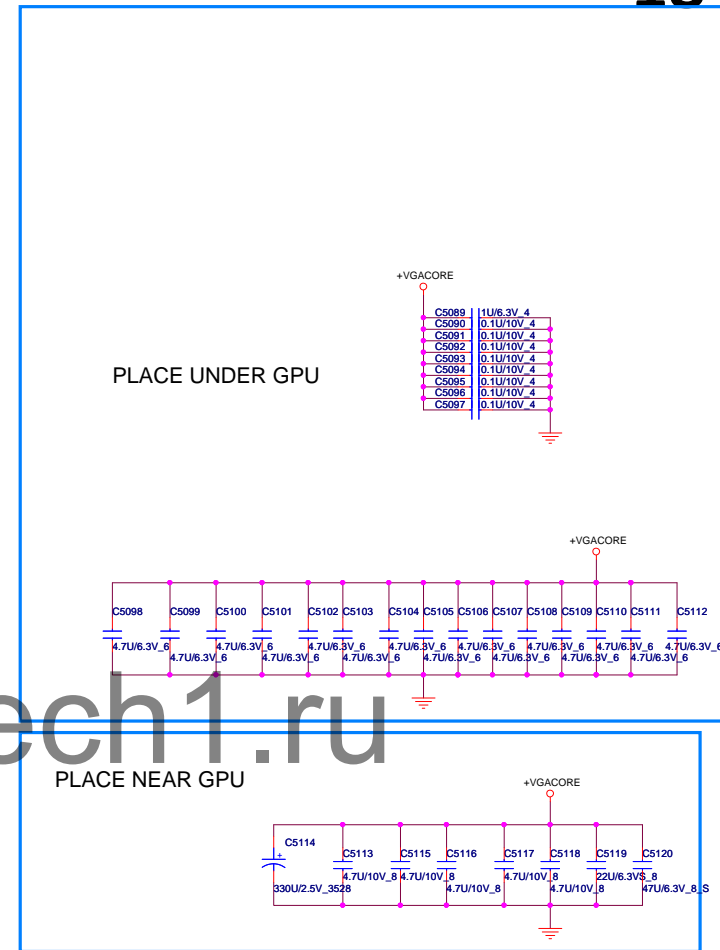
PROJECT : JW2

Quanta Computer Inc.

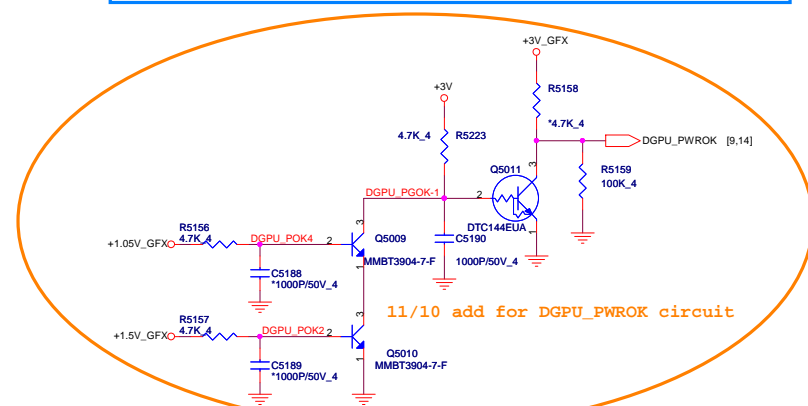
Size Custom Document Number
DGPU 4/5 (MIO/GPIO)

Date: Wednesday, November 02, 2011 Sheet

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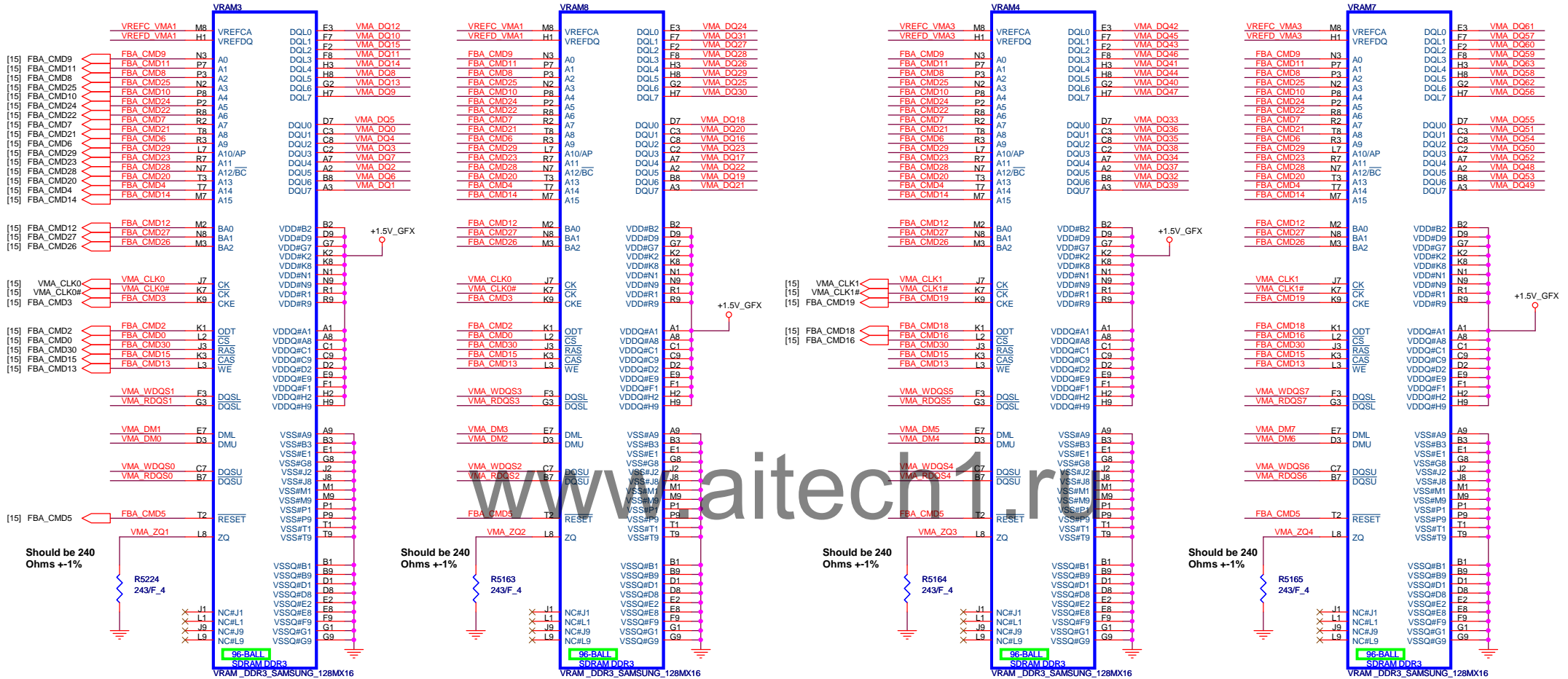
for meet Power down sequence for +3V_GFX



900MHz VRAM size:
 Samsung 64Mx16, P/N = AKD5EGGT500
 Samsung 128Mx16, P/N = AKD5MGWT500
 Hynix 64Mx16, P/N = AKD5LZWTW02
 Hynix 128Mx16, P/N = AKD5MGWTW00

[15] VMA_DQ[63..0]
 [15] VMA_DM[7..0]
 [15] VMA_WDQS[7..0]
 [15] VMA_RDQS[7..0]

CHANNEL A: 256MB/512MB DDR3

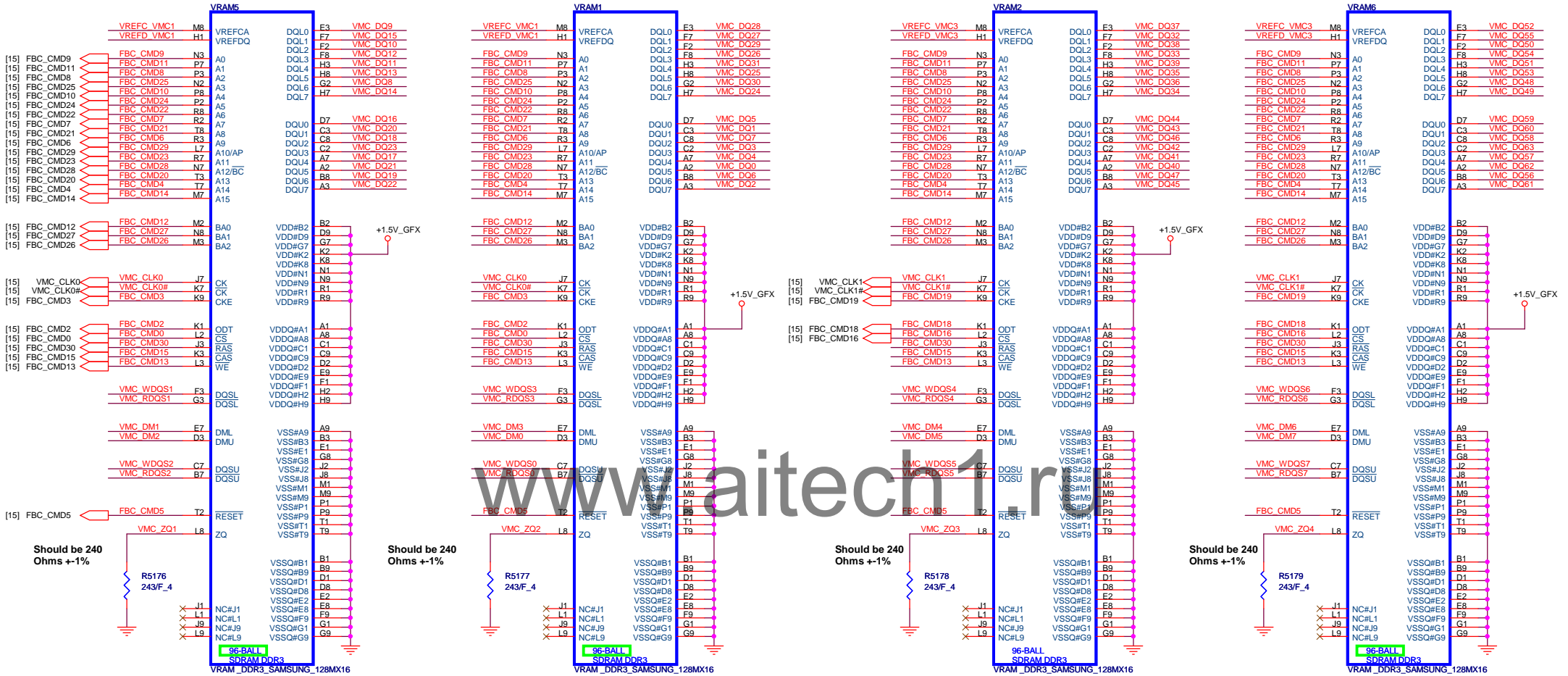


Fermi : Change to 160 ohm
 1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
 2 : CS11622PB07 ,RES CHIP 162 1/16W +-1%(0402)

Fermi : Change to 160 ohm
 1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
 2 : CS11622PB07 ,RES CHIP 162 1/16W +-1%(0402)

[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]

CHANNEL B: 256MB/512MB DDR3

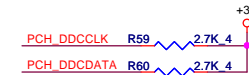
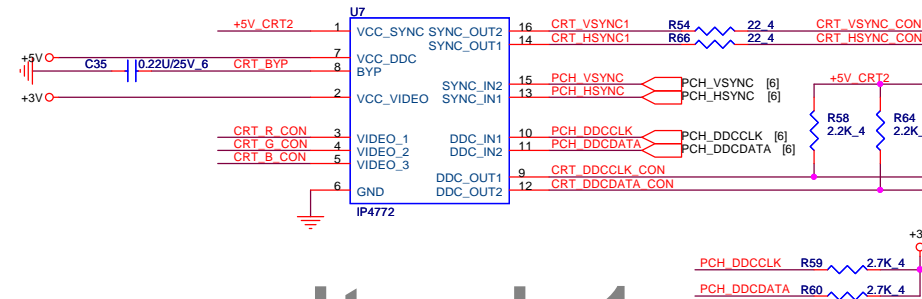
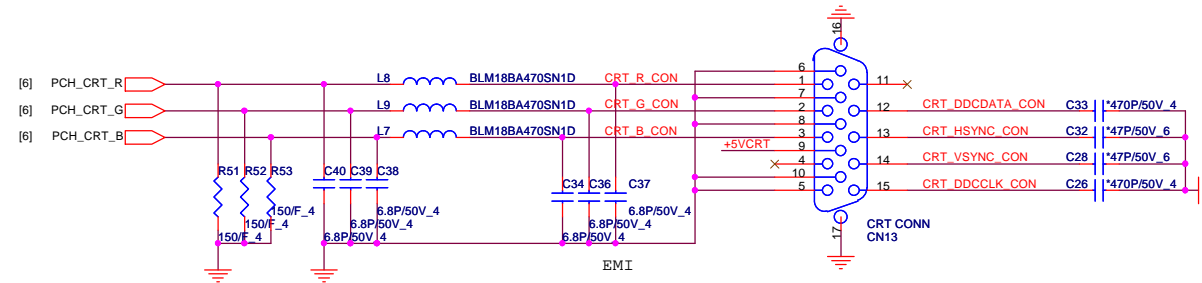
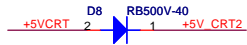
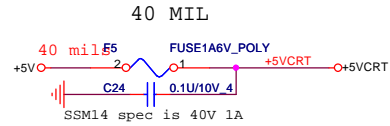


Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

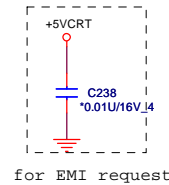
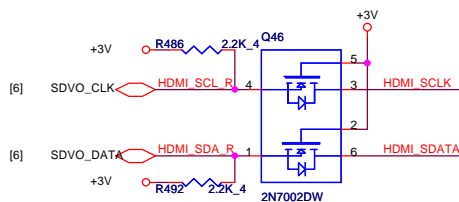
900MHz VRAM size:
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5MGWTW00

CRT PORT



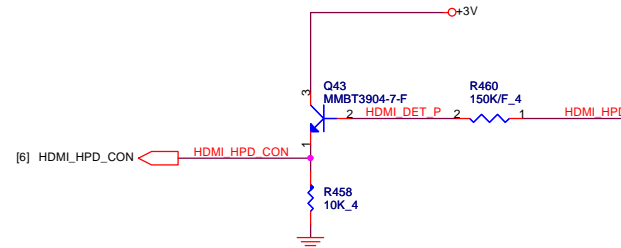
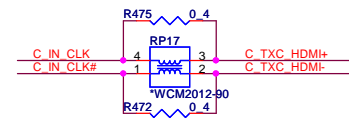
www.aitech1.ru

HDMI SMBus Isolation

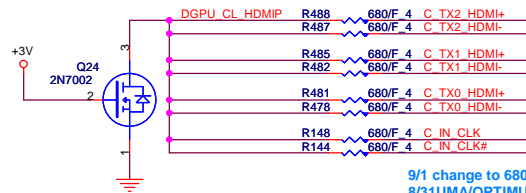
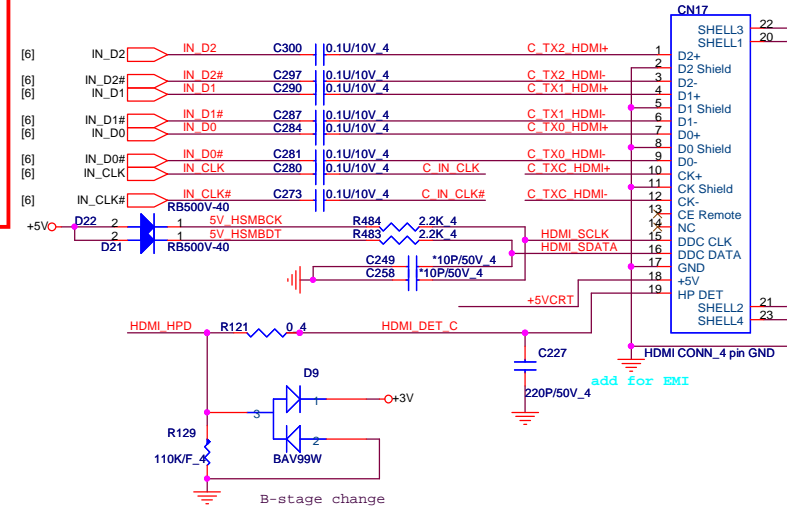


EMI Solution

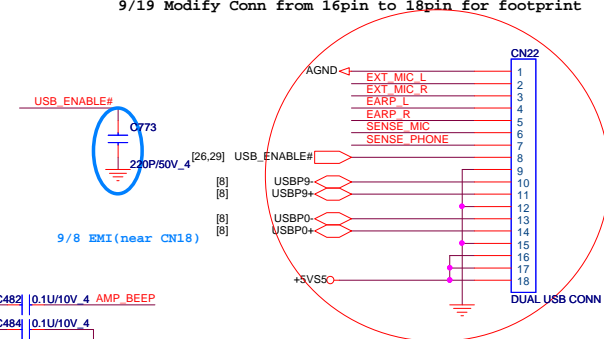
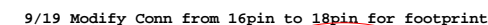
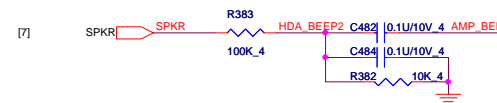
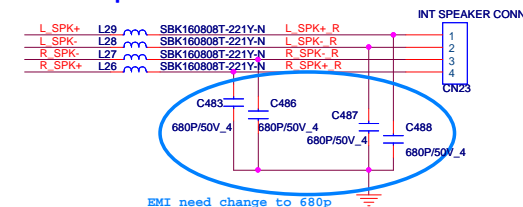
C TX2 HDMI+	R165	0.4	C TX2 HDMI-
C TX1 HDMI+	R159	0.4	C TX1 HDMI-
C TX0 HDMI+	R153	0.4	C TX0 HDMI-
C IN_CLK	R147	0.4	C IN_CLK#

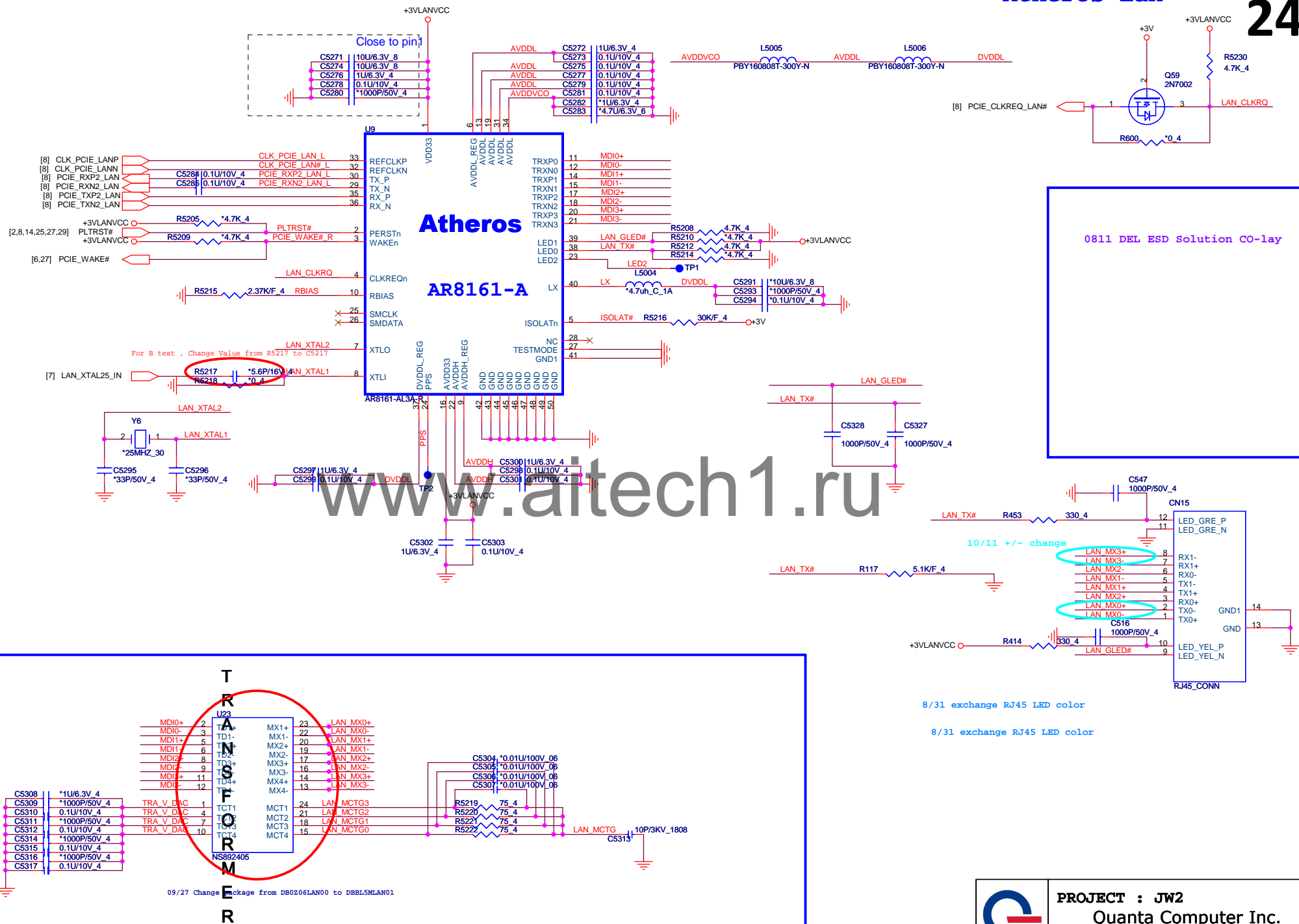


HDMI PORT



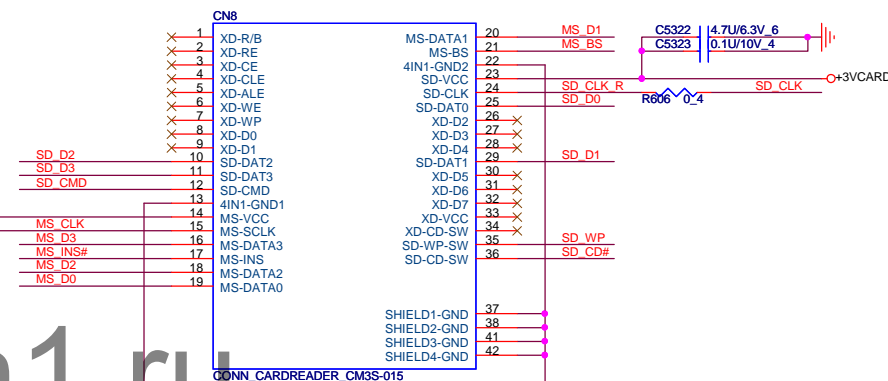
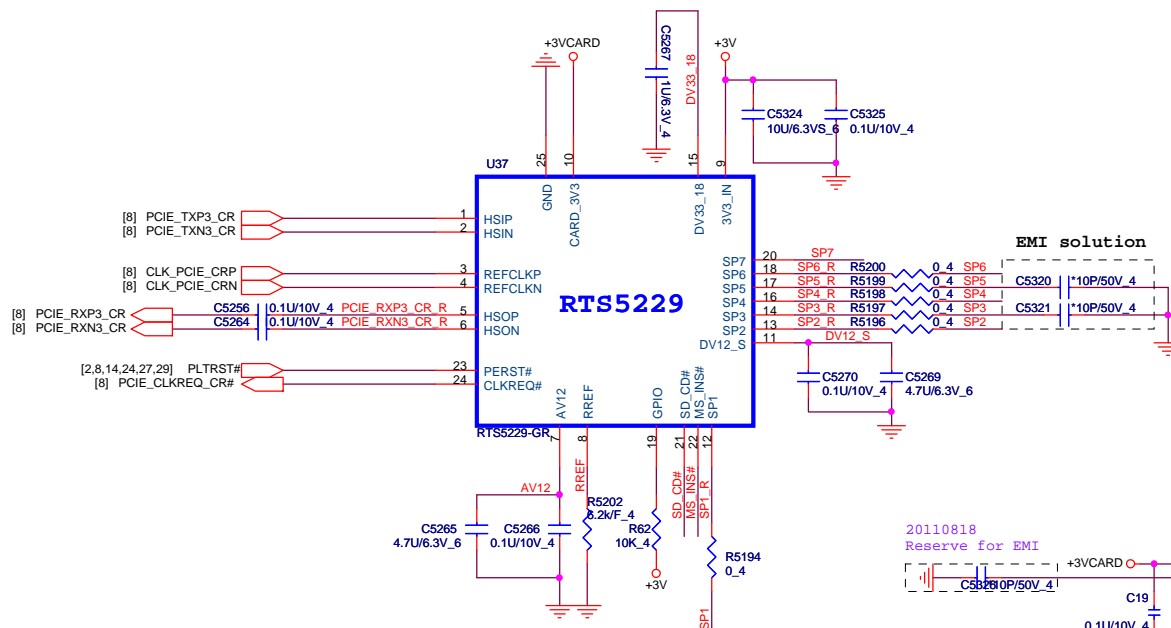
9/1 change to 680ohm
8/31UMA/OPTIMUS-680 ohm, DISCRETE-499 ohm



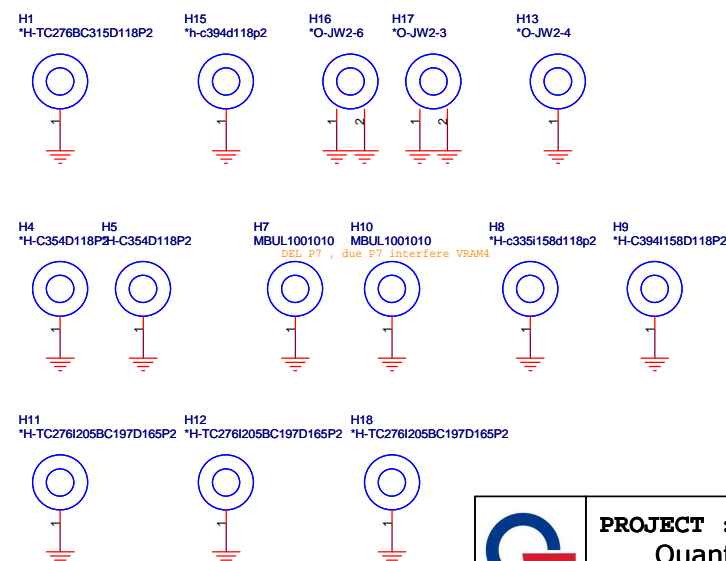


EMI Solution
Please help to close to connector

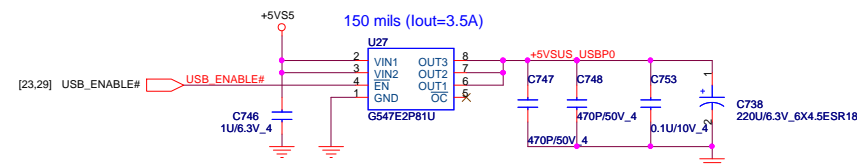
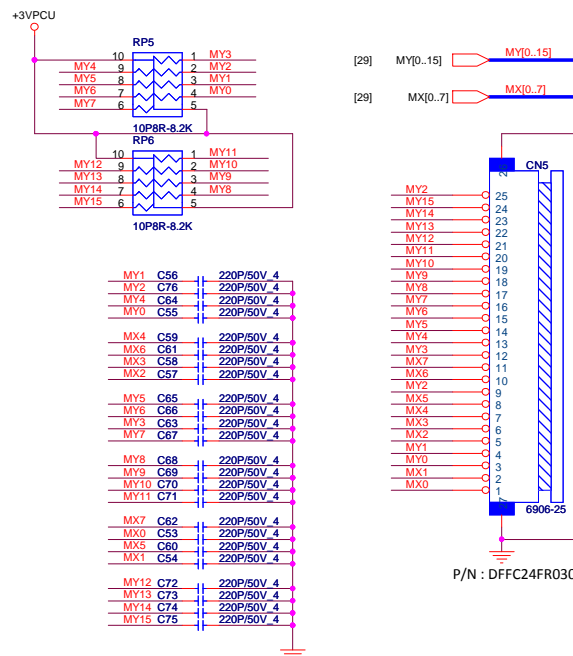
The diagram shows six signal lines for an SD card: SD_CMD, SD_D0, SD_D1, SD_D2, SD_D3, and SD_CLK. Each line is connected to a capacitor (C5257 to C5262) which is then connected to ground. The capacitors are labeled with their values: *5.6P/16V_4. The text 'EMI Solution' and 'Please help to close to connector' is written above the capacitors.



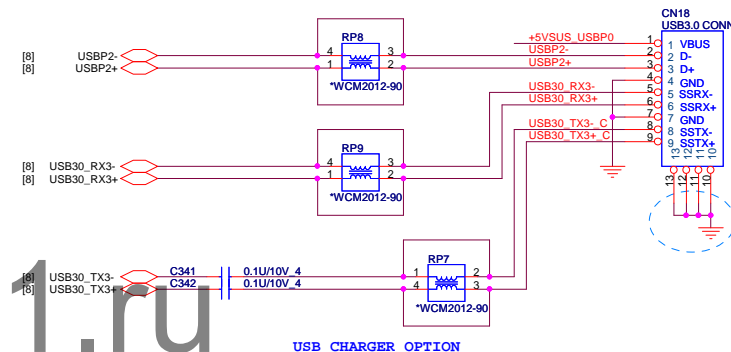
2. C5265, C5202 close to U37 pin7
3. C1021, C1022 close to U37 pin11
4. C1089, C1090 close to U37 pin9
5. C1019 close to U37 pin15
6. C1026, C1027 close to CN27 pin11
7. C1025 close to CN27 pin4



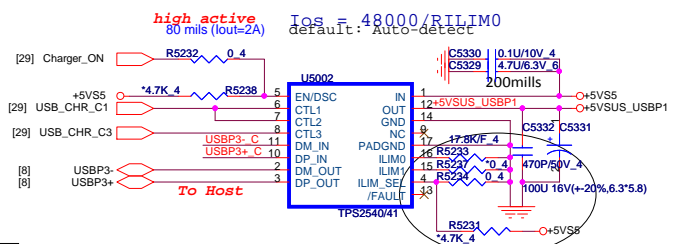
Keyboard Connector



USB3.0 X 2/USB2.0 COMBO **USB 3.0**



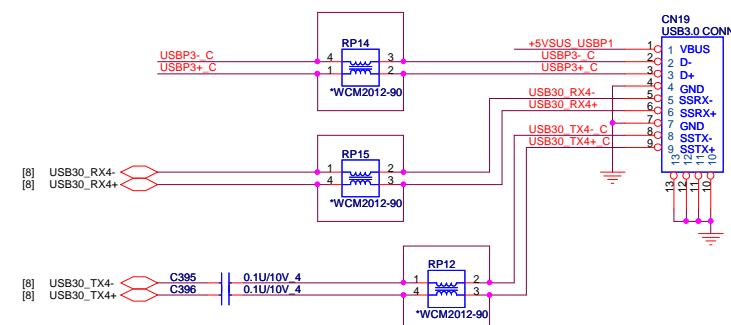
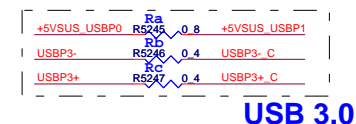
Charger USB



CTL1	CTL2	CTL3	TPS2540 Control Truth Table
0	0	0	Out Discharge ,Power switch OFF
0	X	1	Dedicated charging port, auto-detect
X	1	0	Standard downstream port, USB 2.0
1	1	1	Mode(SDP) Charging downstream port, BC1.2

LGE SPEC	S0/S3		S4/S5	
	AC Mode	DC Mode	AC Mode	DC Mode
change mode	CDP	CDP	DCP	DCP
user define and wake up		SDP		OFF

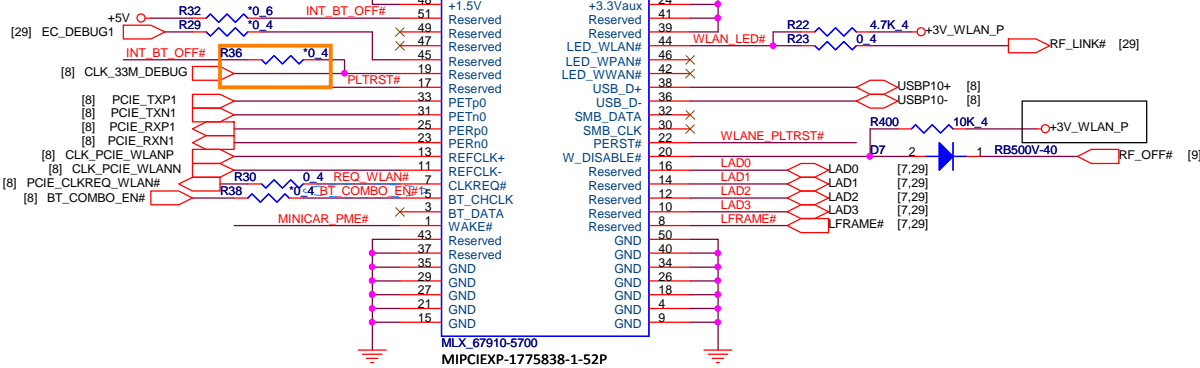
U5002	Ra	Rb	Rc
STUFF	UNSTUFF	UNSTUFF	UNSTUFF
UNSTUFF	STUFF	STUFF	STUFF



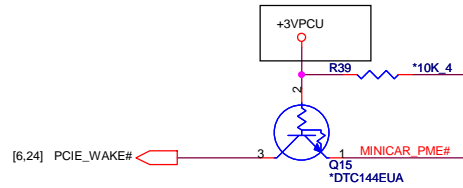
Mini Card WLAN/BT(Optional)

EC debug pin

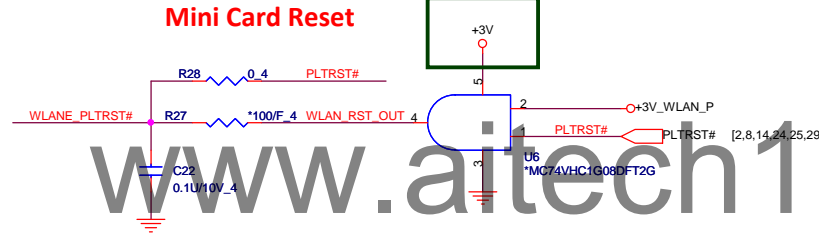
Intel DG request



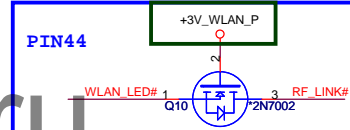
Support Wake Function(Reserve)



Mini Card Reset



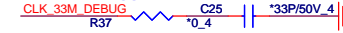
Avoid leakage issue



1GE mini-pcie power status

WLAN	Bluetooth	+3V_WLAN_P
Radio-ON	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

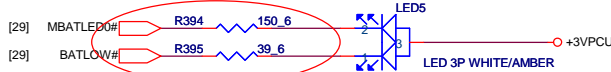
For EMI Suggestion



LED Status

9/1 Change LED from stand up to lie down

(White)

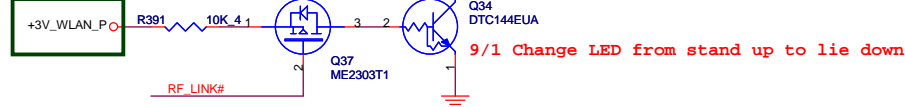
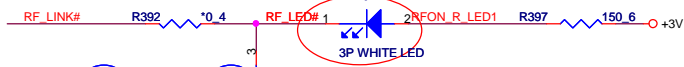


(Orange)

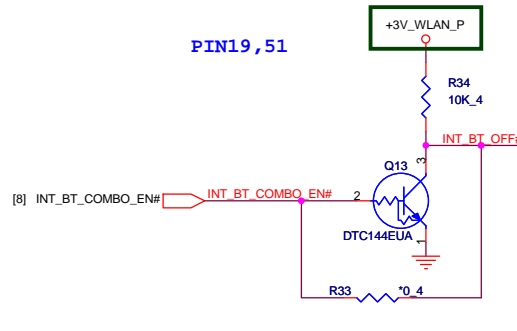
(White)



9/1 Change LED from stand up to lie down (White)



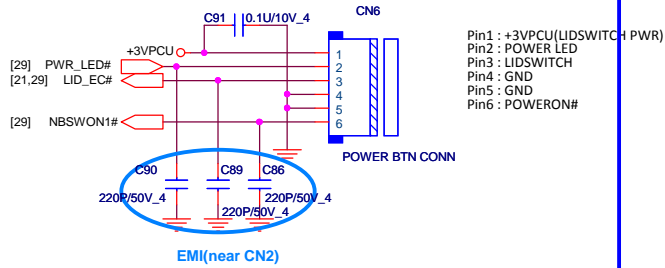
PIN19, 51



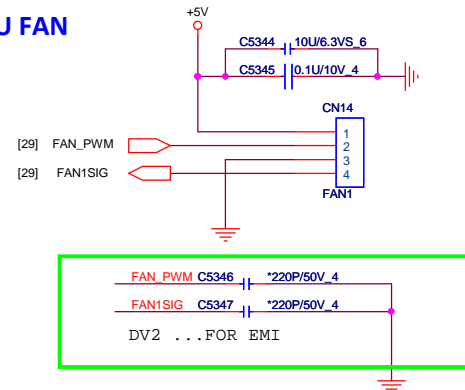
9/4 Intel COMBO card control circuit

- 1.add R1001,R1002,Q1001
- 2.add net name"INT_BT_COMBO_EN#" -> "INT_BT_OFF#"

Power Button Connector

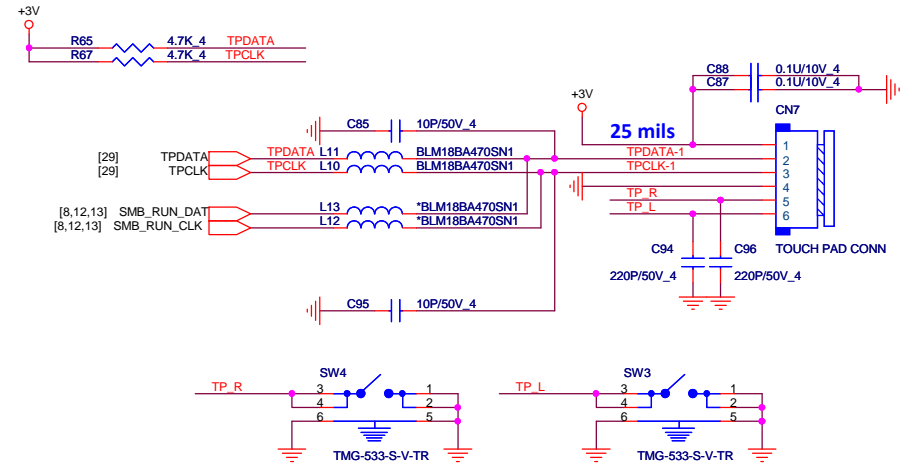


CPU FAN

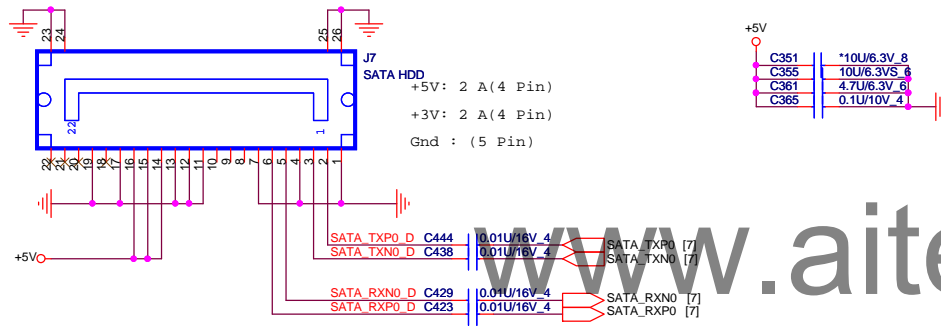


Touch Pad Connector

B-stage change footprint to BL121-12R-TAND-12P-L



SATA HDD Connector

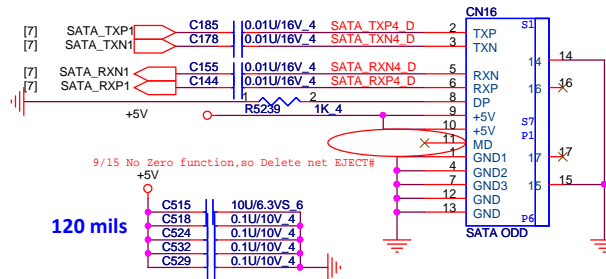


Finger Print Connector

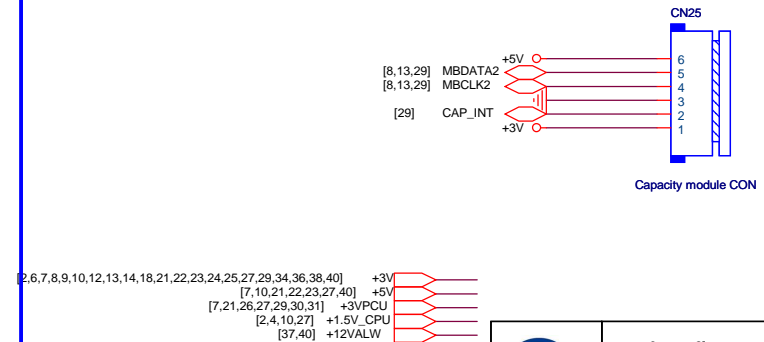
SATA ODD Connector

0812 ODD ZERO PWR DEL

20110818 ODD_PRSENT DEL



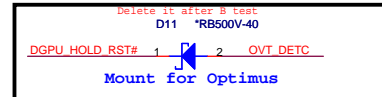
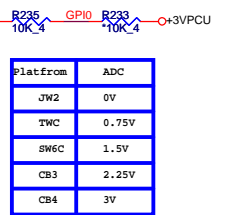
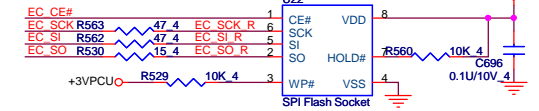
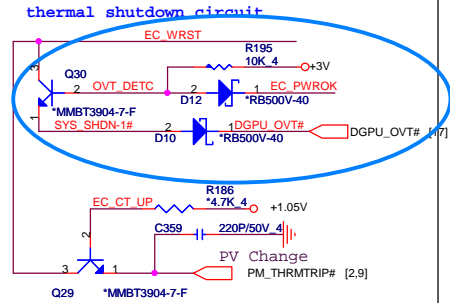
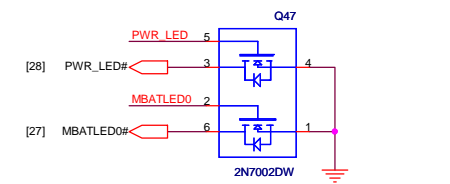
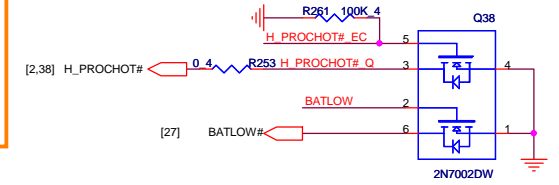
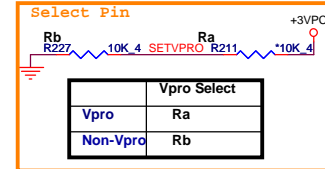
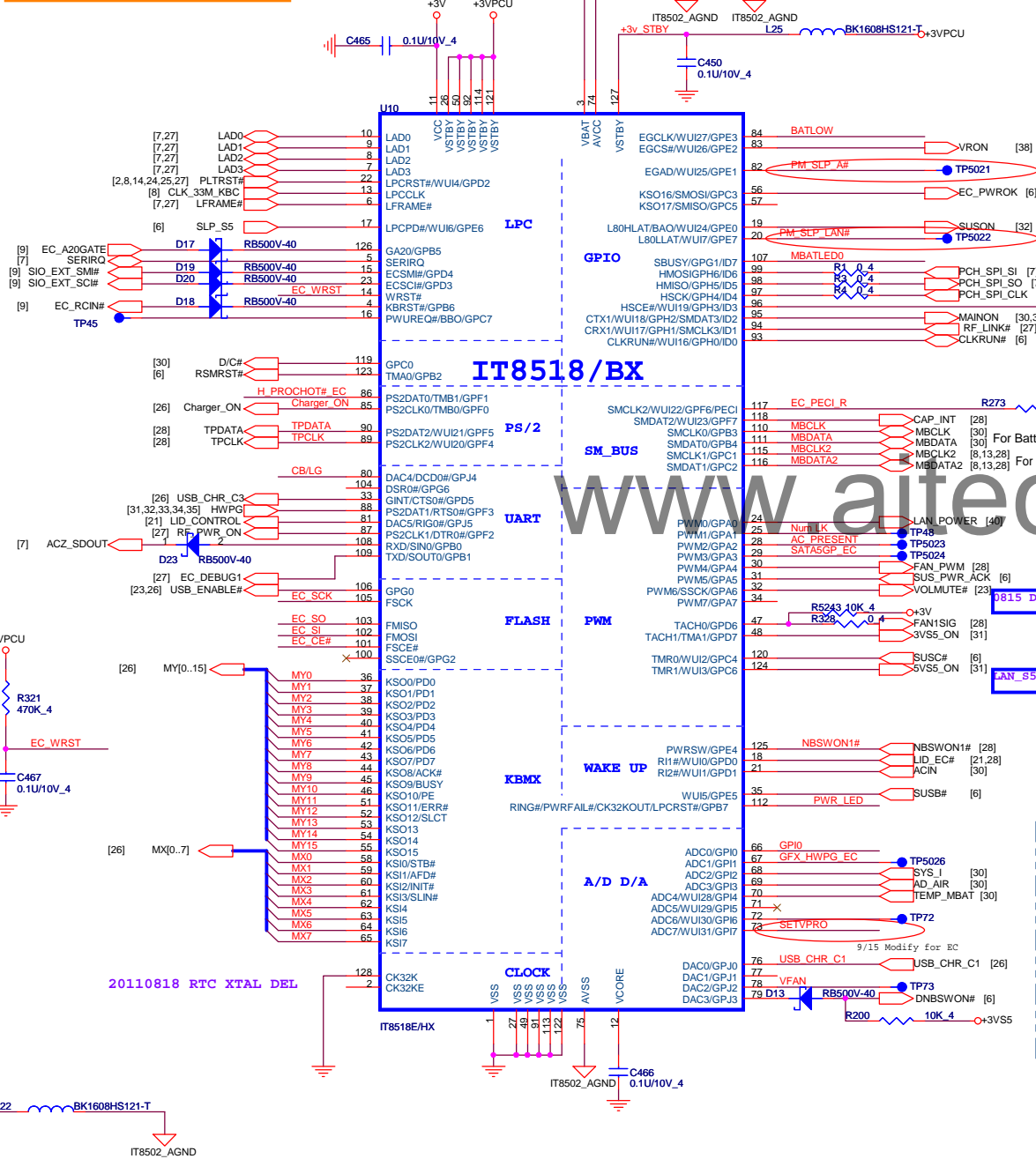
Capacity module Connector



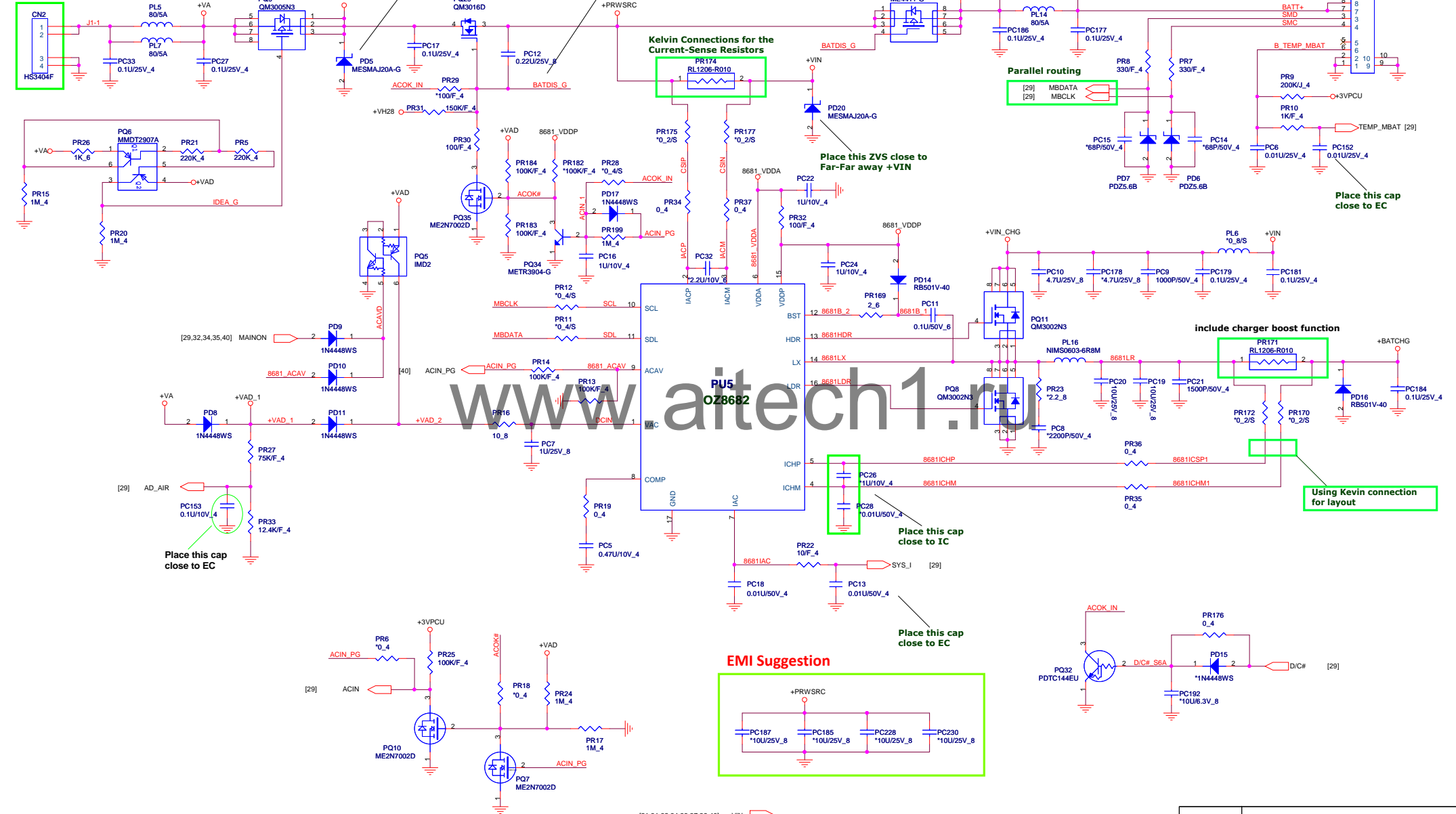
PROJECT : JW2
Quanta Computer Inc.

Size Custom	Document Number SATA HDD/ODD/MSATA CONN	Rev/D A
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Date: Wednesday, November 02, 2011 Sheet 28 of 40

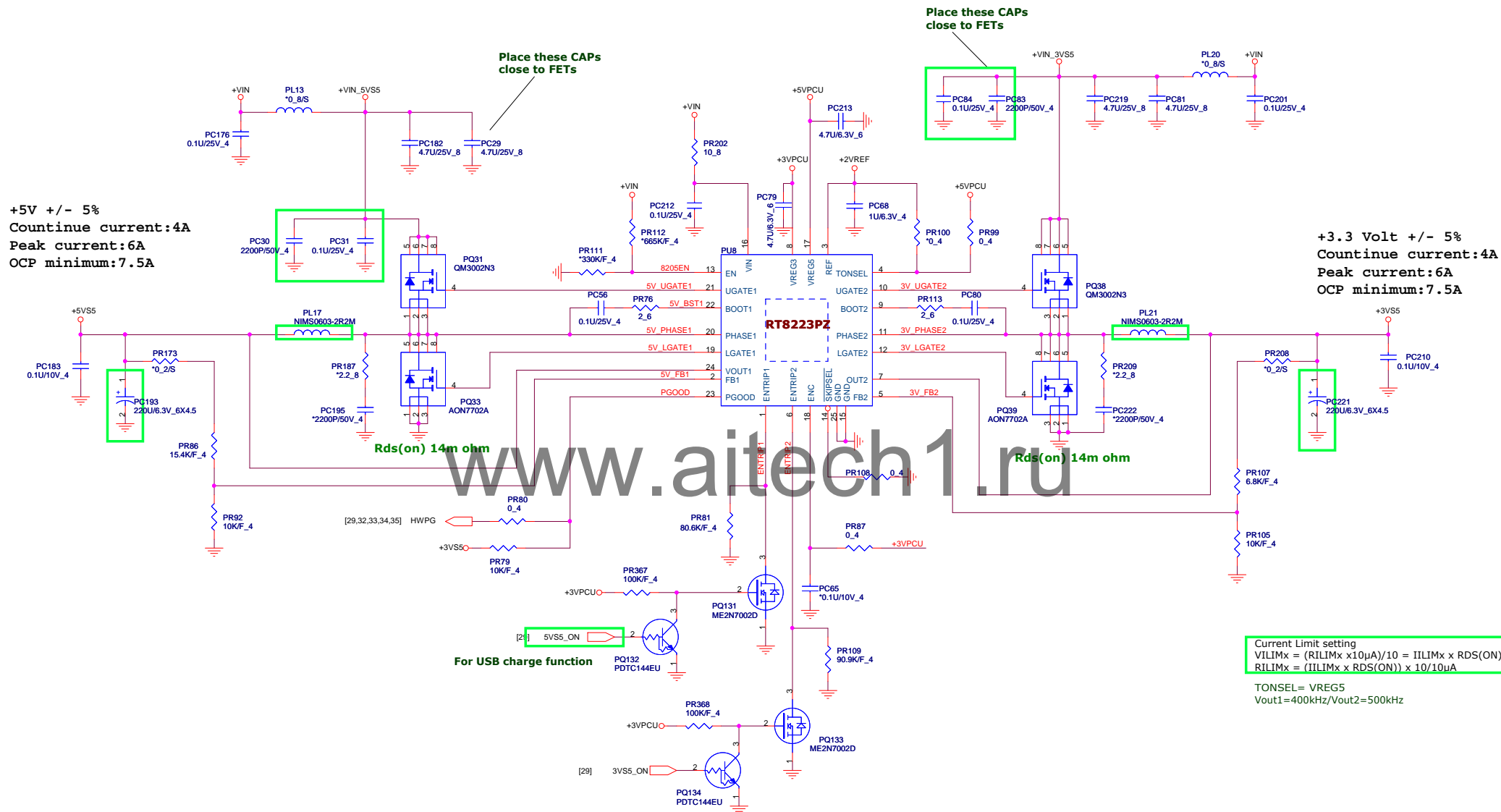


TOP DC_JACK
90W/4.75A



[21,31,32,34,36,37,39,40]	+VIN	
[40]	+VAD	
[40]	+VH28	
[40]	+VAD ₁	
[7,21,26,27,28,29,31]	+3VPCU	

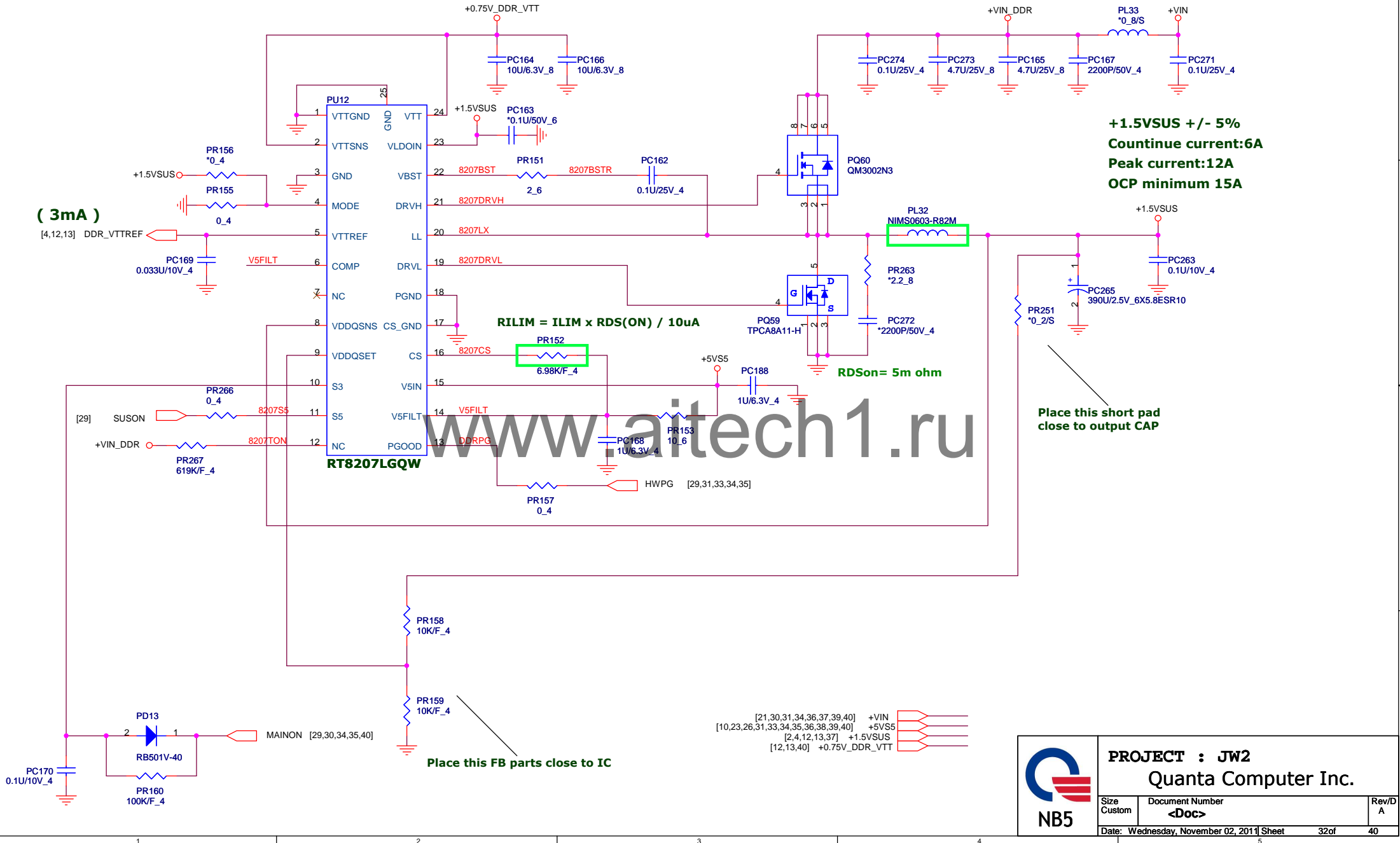
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW




[21,30,32,34,36,37,39,40] +VIN
 [6,7,8,9,10,23,34,35,37,40] +3VSS
 [10,23,26,32,33,34,35,36,38,39,40] +5VSS
 [7,21,26,27,28,29,30] +3VPCU

(VTT/2A)

(3mA)

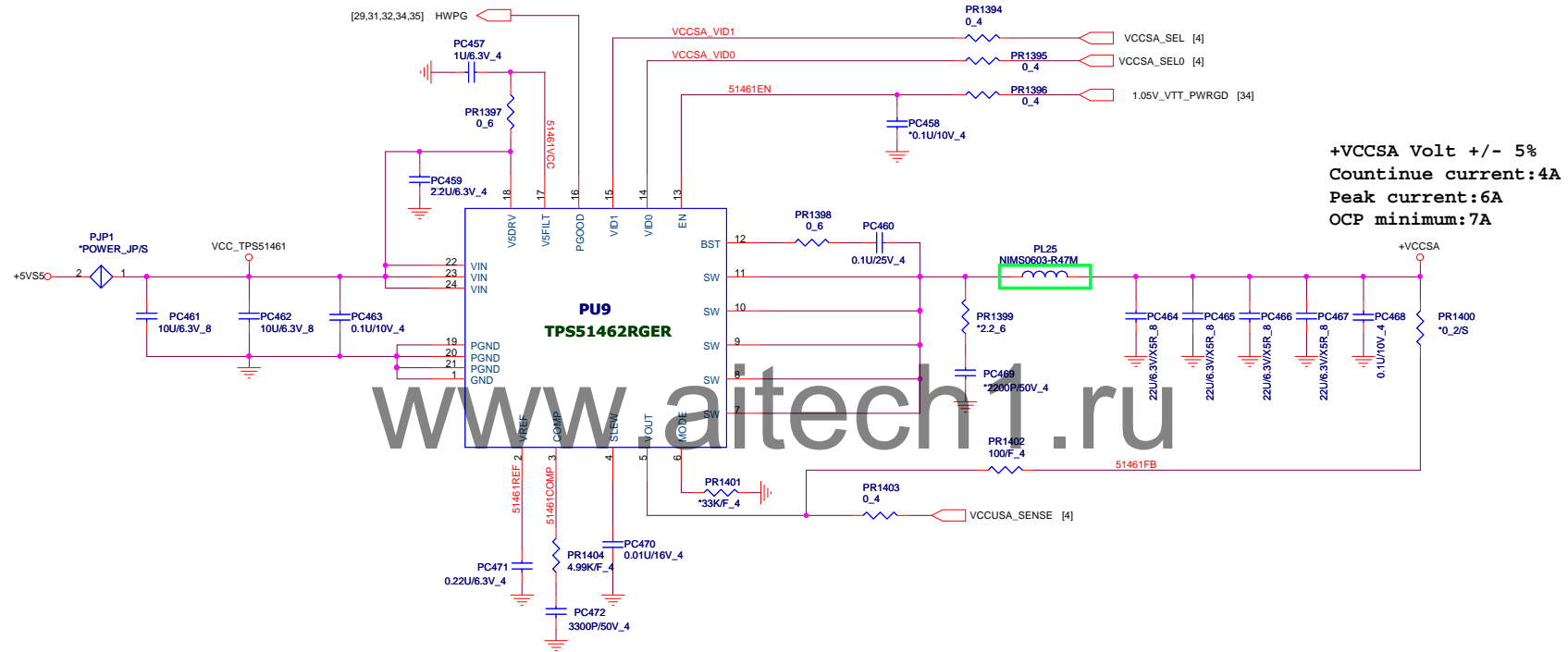


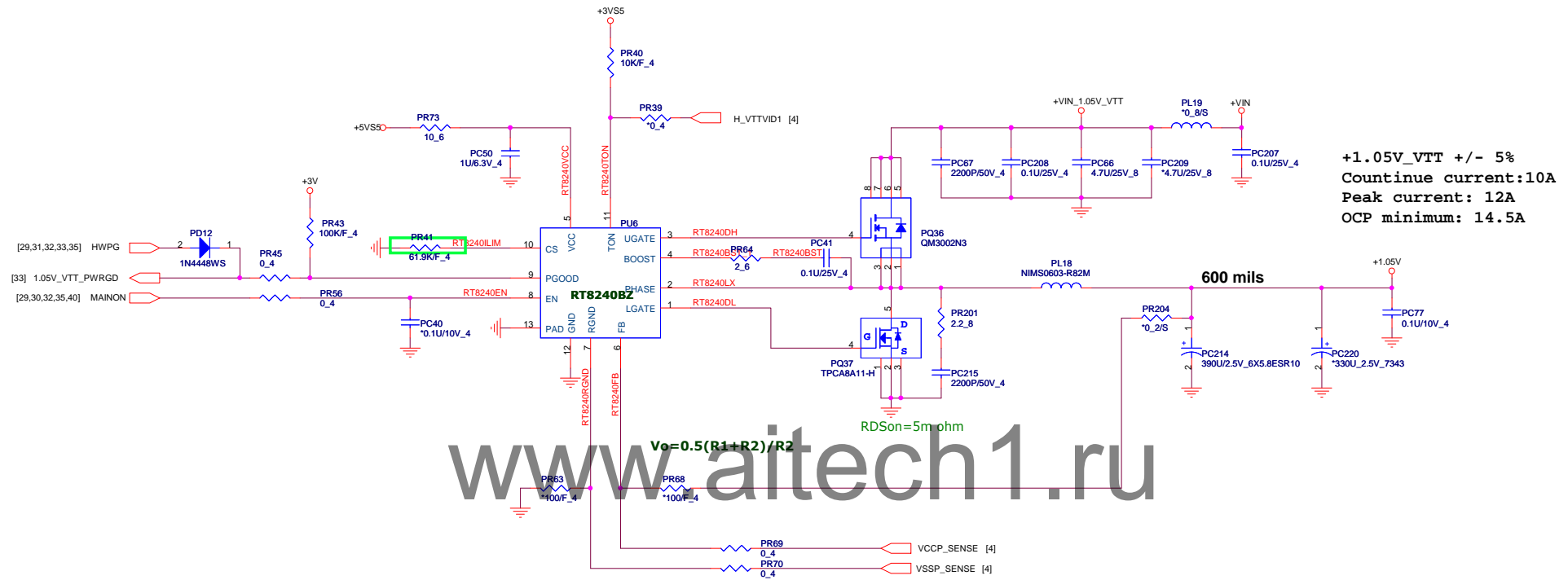
+1.5VSUS +/- 5%
Countinue current:6A
Peak current:12A
OCp minimum 15A

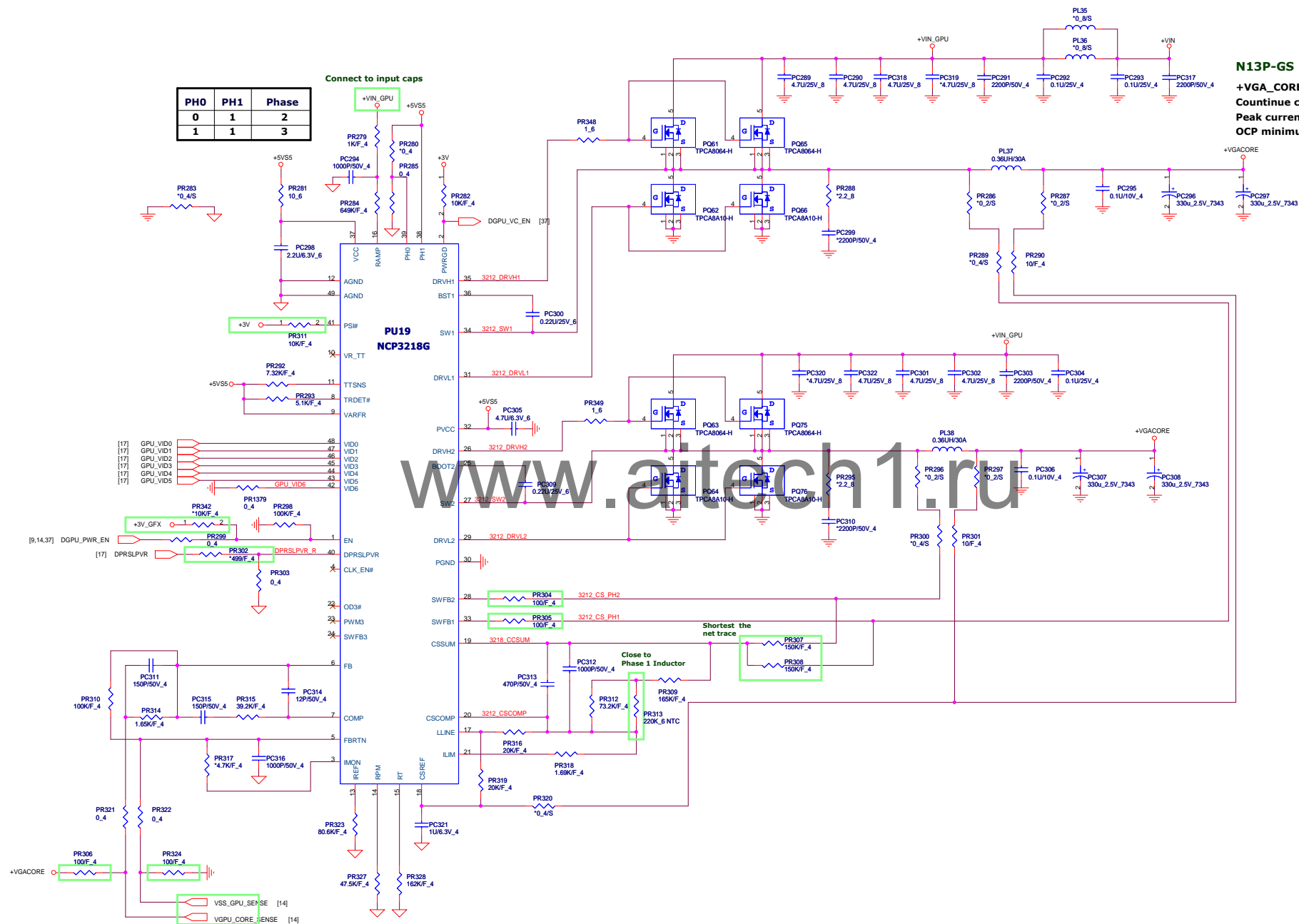
 NB5	PROJECT : JW2 Quanta Computer Inc.		
	Size Custom	Document Number <Doc>	Rev/D A
	Date: Wednesday, November 02, 2011 Sheet 32 of 40		

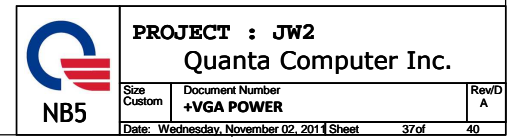
CPU system agent
voltage slew rate of 0.5 -10 mV/ μ s

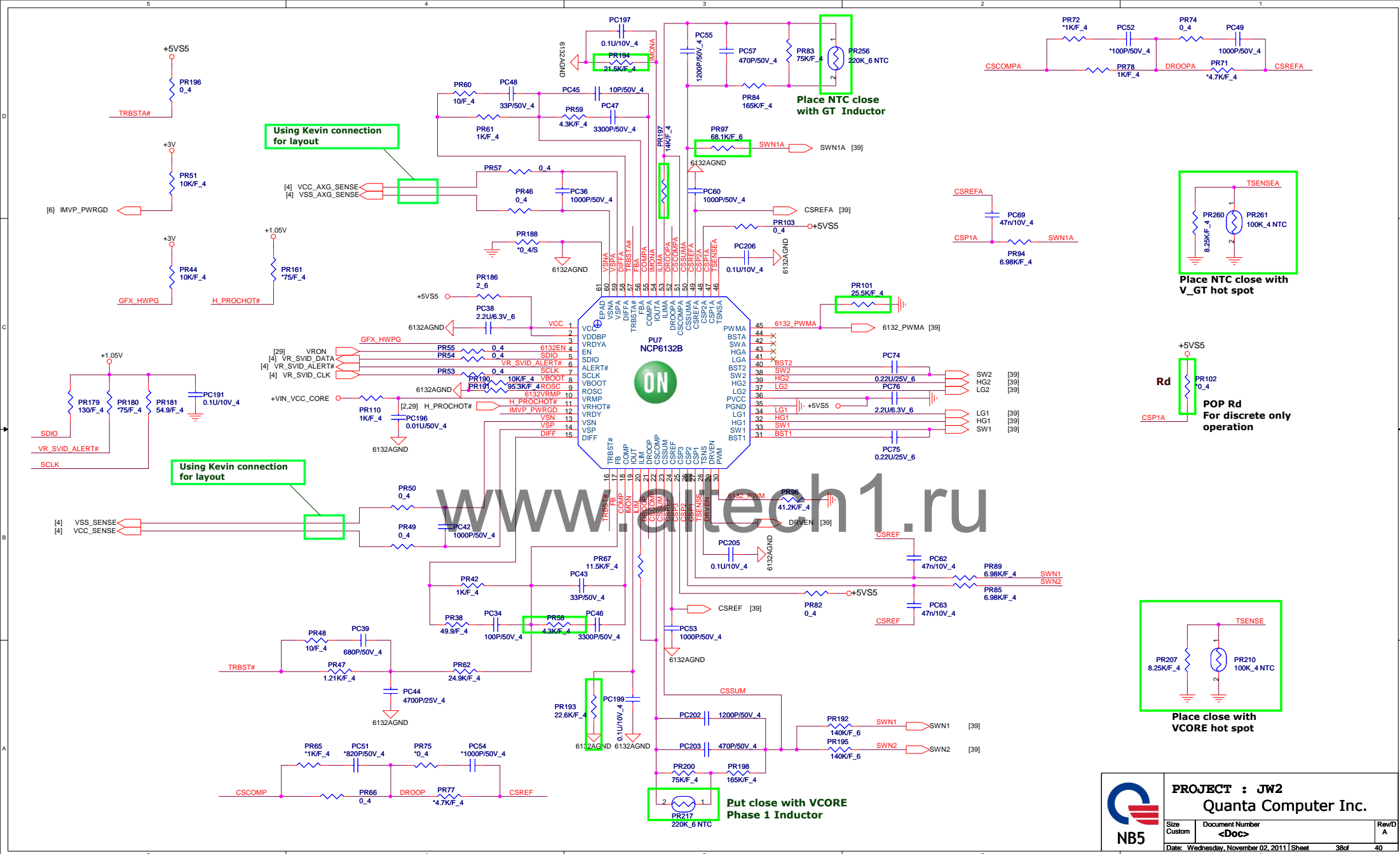
SELO	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V











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